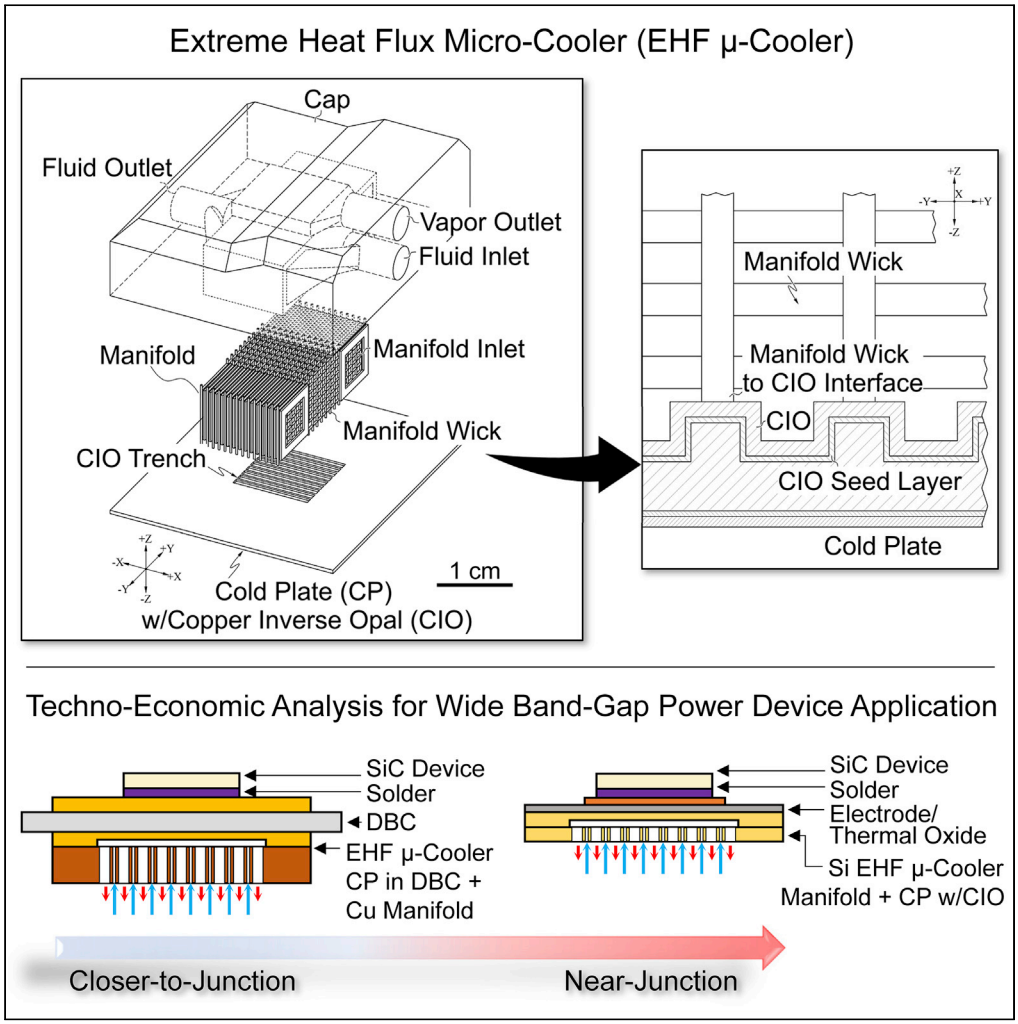
iScience

CellPress
OPEN ACCESS

Article

Techno-economic feasibility analysis of an extreme heat flux micro-cooler



Ercan M. Dede, Chi Zhang, Qianying Wu, ..., Kenneth E. Goodson, Roman Giglio, Mehdi Asheghi

eric.dede@toyota.com (E.M.D.)
masheghi@stanford.edu (M.A.)

Highlights

Highly efficient power electronics will have a major impact on worldwide energy use

Thermal management of power devices is one key to realizing related energy savings

Techno-economic analysis is done for a near-junction extreme heat flux micro-cooler

The micro-cooler is estimated to be performance/cost competitive in the marketplace

Dede et al., iScience 26, 105812
January 20, 2023
https://doi.org/10.1016/j.isci.2022.105812

iScience

CellPress
OPEN ACCESS

Article

Techno-economic feasibility analysis of an extreme heat flux micro-cooler

Ercan M. Dede,[1,7,*] Chi Zhang,[2,6] Qianying Wu,[2] Neda Seyedhassantehrani,[4] Muhammad Shattique,[3] Souvik Roy,[4] James W. Palko,[4] Sreekant Narumanchi,[5] Bidzina Kekelia,[5] Sougata Hazra,[2] Kenneth E. Goodson,[2] Roman Giglio,[4] and Mehdi Asheghi[2,*]

SUMMARY

An estimated 70% of the electricity in the United States currently passes through power conversion electronics, and this percentage is projected to increase eventually to up to 100%. At a global scale, wide adoption of highly efficient power electronics technologies is thus anticipated to have a major impact on worldwide energy consumption. As described in this perspective, for power conversion, outstanding thermal management for semiconductor devices is one key to unlocking this potentially massive energy savings. Integrated microscale cooling has been positively identified for such thermal management of future high-heat-flux, i.e., 1 kW/cm^2, wide-bandgap (WBG) semiconductor devices. In this work, we connect this advanced cooling approach to the energy impact of using WBG devices and further present a techno-economic analysis to clarify the projected status of performance, manufacturing approaches, fabrication costs, and remaining barriers to the adoption of such cooling technology.

INTRODUCTION

Utilization of power electronics between the point of electricity generation and point of use is prevalent in the United States,[1] reflecting a global trend.[2] The level of usage of power electronics for electric power transfer applications is expected to steadily increase from the current 70% to ~100% over time given widespread usage in motor drives, data centers, distributed/renewable energy systems, aerospace, and automotive vehicles.[2] Next-generation wide-bandgap (WBG) power semiconductor devices are an enabling technology for increased energy efficiency across this broad range of sectors.[3,4] Compared to established silicon (Si)-based power semiconductor devices, silicon carbide (SiC) and gallium nitride (GaN) WBG power devices offer a range of benefits including lower on-resistance, higher breakdown voltage, and low conduction losses. Power electronics systems with WBG devices can further operate at higher power, higher switching frequency, higher voltage, and higher efficiency in new circuit topologies,[5,6] which additionally allows for downsizing (i.e., increased volumetric and/or gravimetric power density) of the electronics package.[7] Perhaps most critically, through the adoption of WBG power devices and systems, significant energy savings of 10-50% may be realized depending on the application, and some examples include electric motors with variable speed drives,[8] electrified vehicles,[7] and more electric aircraft,[9] to name a few. In the U.S. ground-based transportation sector alone, well-to-wheel analysis of the adoption of WBG power semiconductor devices in power electronics projects a potential 2-20 billion GJ energy savings impact waiting to be realized in the 2015-2050 timeframe.[10] Extrapolated to the global scale and across industries, this has enormous implications for the world and the environment.

In practice, realizing the increased power density of power electronics systems that employ WBG semiconductor devices poses a host of technical issues ranging from electrical circuit topology considerations to advanced materials development, and importantly, thermal management challenges. Regarding the latter point, which is the focus of this techno-economic analysis (TEA), heat fluxes for 0.25 cm^2 to 3 cm^2 individual power semiconductor devices, or large-size arrays of small devices, are anticipated to approach or exceed q'' = 1 kW/cm^2 in the future due to power dissipated in the form of heat close to the device junction. While single-phase liquid cooling[11,12] positioned remotely from a Si power semiconductor device in an electronics package is common, the potential 2× to 10× higher heat fluxes of smaller WBG power devices with aggressive power dissipation levels present a need for breakthrough thermal management solutions.

[1]Electronics Research Department, Toyota Research Institute of North America, Ann Arbor, MI, USA

[2]Department of Mechanical Engineering, Stanford University, Stanford, CA, USA

[3]Department of Materials and Biomaterials Science and Engineering, University of California-Merced, Merced, CA, USA

[4]Department of Mechanical Engineering, University of California-Merced, Merced, CA, USA

[5]National Renewable Energy Laboratory, Golden, CO, USA

[6]School of Integrated Circuits, Peking University, Beijing 100871, P.R. China

[7]Lead contact

*Correspondence: eric.dede@toyota.com (E.M.D.), masheghi@stanford.edu (M.A.)

https://doi.org/10.1016/j.isci.2022.105812

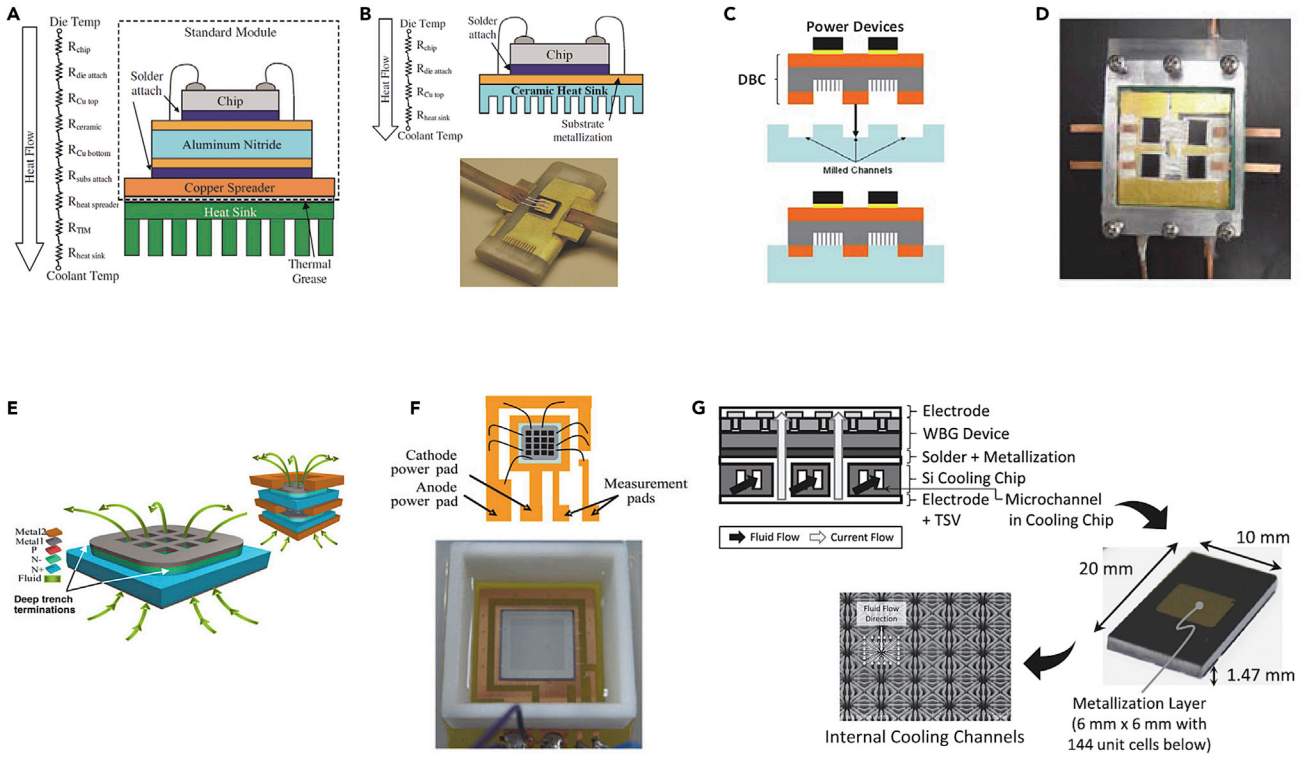


Figure 1. Near-junction cooling concepts for power semiconductor devices

(A and B) Conventional power electronics module schematic for vertical current power device with "remote cooling" heat sink, (A), where each layer adds thermal resistance between source and sink. Modified package with reduced thermal resistance, (B), where electrical isolation is provided by the AlN ceramic heat sink; fabricated cooler shown in lower image with die-bonded SiC diode. © [2008] IEEE. Reprinted, with permission, from Jankowski et al.[14]

(C and D) Manifold microchannel (MMC) heat sink structure, (C), fabricated in the AlN layer of a DBC substrate for power electronics packaging. Fabricated prototype, (D). © [2010] IEEE. Reprinted, with permission, from Sharar et al.[16]

(E and F) Concept for microscale cooling integrated into drift region, (E), of vertical power diode. Schematic and prototype vertical power diode device, (F). © [2013] IEEE. Reprinted, with permission, from Vladimirova et al.[18]

(G) Vertical current device power package concept, on upper left, with microchannels in separate chip-scale cooler. Image of fabricated Si cooling chip, on right. Perspective SEM image of first layer of microchannel 500 μm × 500 μm unit cell array, at lower center. Reprinted from Zhou et al.[21] © [2019], with permission from Elsevier.

Accordingly, near-junction cooling has been proposed as an answer with high potential to move beyond this "remote cooling" convention.[13]

Here, we briefly review prior work on the experimental demonstration of near-junction cooling to better understand realistic state-of-the-art integration concepts. With respect to power electronics, early effort to move past the "remote cooling" paradigm is found in the work from the Army Research Lab (ARL),[14] where the number of layers in a standard power electronics module was reduced by utilizing an aluminum nitride (AlN) ceramic cooler; see Figures 1A and 1B. The AlN cooler allows for the elimination of substrate attach (e.g., solder bond) and thermal interface material (TIM) layers of the package, while providing the kilovolt (kV) level electrical isolation necessary for a functional vertical current power semiconductor device. Experimental testing of devices like those shown in Figure 1B revealed total packaged device unit thermal resistance values of <0.175 K-cm^2/W with pressure drop of the supplied single-phase coolant on the order of 5 kPa.[14] This work was extended by ARL to devices packaged using a manifold microchannel (MMC) heat sink[15] configuration fabricated in the AlN ceramic layer of a direct-bond-copper (DBC) substrate,[16] as shown conceptually and in prototype form in Figures 1C and 1D, respectively. An advantage in employing a DBC (or similar) substrate is that it is a common approach to electrical isolation and packaging in power electronics applications.[17] However, more aggressive cooling strategies are envisioned, and an example of integrating the cooling function into the drift region of an active power device, Figure 1E, has been additionally proposed.[18] While the concept was anticipated through numerical modeling to have good thermal performance and non-detrimental effects on the electrical characteristics of the device, experimental testing of

the prototype, Figure 1F, with dielectric coolant (for electrical isolation) showed ~6× higher-than-expected thermal resistance with cracks in the device metallization layer leading to a non-homogeneous current distribution plus hot spots during operation. These experimental results[18] highlight multiphysics performance, reliability, and ultimately associated cost challenges related to modifying the actual power device structure itself. Another somewhat related approach not illustrated in Figure 1 is immersion cooling, and several variations of immersion cooling using dielectric fluids for high-power electronics have been proposed in the past.[19] Despite recent resurgence of this topic, reliability concerns (e.g., fluid leakage/sloshing, material compatibility, boiling induced erosion/corrosion to terminals/interconnects and packaging)[20] persist. Thus, the reliability plus complexity and cost of an immersion cooling thermal management system may still be a primary limitation for harsh-environment mobility-related applications when compared with other near-junction solutions. Considering this, a chip-scale cooling strategy[21,22] like that in Figure 1G may provide balance between aggressive near-junction thermal management, electrical isolation, and minimal impact to the long-term reliability of an active vertical current power device structure plus package. Practical cooling of aggressive device heat fluxes is then accessible using such an approach.

In this perspective, and in support of wide adoption of WBG power semiconductor devices for increased system energy efficiency, we address an important gap in the literature related to the TEA of near-junction cooling technology. Based on the prior introduction, we first summarize candidate electronics package configurations for integrating an extreme-heat-flux micro-cooler (EHF μ-Cooler) near to the junction of a power electronics package. Here, we note that the EHF μ-Cooler concept is to some degree related to a range of capillary-driven two-phase "remote" solutions found in the literature including vapor chambers[23,24] and hybrid cooling,[25] which confirm promise toward handling aggressive device heat fluxes through structured design of fluid wicking paths in multiple dimensions. Thus, performance analyses for down-selected packages that employ an EHF μ-Cooler are presented utilizing associated numerical modeling results. The TEA proceeds with a description of material and methods as inputs to fabrication process flows for two EHF μ-Cooler candidate configurations. Estimated cost results for low-volume production runs of these cooler configurations are presented along with a summary of recent fabrication progress. A discussion of market recommendations and barriers to adoption is provided before conclusions along with limitations of the present study.

RESULTS

Techno-economic analysis model development

A schematic of the EHF μ-Cooler concept is provided in Figure 2A, and this cooler operates in a two-phase (i.e., boiling) heat transfer mode. Three-dimensional (3-D) capillary-force-driven delivery of the single-phase coolant fluid from an inlet to the cold plate wick via a fluid- flow-manifold wick occurs with eventual vapor (and heat) exiting vertically through the cold plate outlet channels. Observe that the cold plate wick comprises a conformal copper inverse opal (CIO) microstructure deposited on to a Si or copper (Cu) cold plate for enhanced two-phase heat transfer at the cold plate heated surface. As discussed at length in wick-level studies,[26] such CIO microstructures, when operating in the two-phase heat transfer regime, are capable of supporting heat fluxes exceeding 1 kW/cm^2. Motivated by cost considerations, two different manifold configurations are considered in this TEA. Specifically, a Si wafer-based manifold structure fabricated using lithography and similar to prior work[22] is discussed along with a lower cost stacked Cu layer-based mesh (or additively manufactured) wick design; see Figure 2A. Depending on the manifold configuration, different EHF μ-Cooler assembly architectures are assumed in the near-junction application package configurations that follow.

Power package configurations

Three feasible packages for a power semiconductor device cooling application are considered. A remote cooling strategy for a double-side-cooled power card structure is shown for reference, Figure 2B, where an all-Cu EHF μ-Cooler replaces a standard cold plate, and the required kV-level electrical isolation for the power device is achieved in standard fashion with silicon nitride (Si_3N_4) ceramic shims. This integration approach is representative of a traction drive application[27] and has as many as four TIM layers, each with relatively high conductive thermal resistance, R_{th_cnd}, between the semiconductor device and cooler.

A second strategy for integrating the EHF μ-Cooler closer to the junction and eliminating numerous TIM layers is illustrated in Figure 2C, where the CIO wick is deposited on to the bottom Cu layer of the package DBC. Here, the AlN layer of the DBC again provides the necessary high-voltage electrical isolation for a

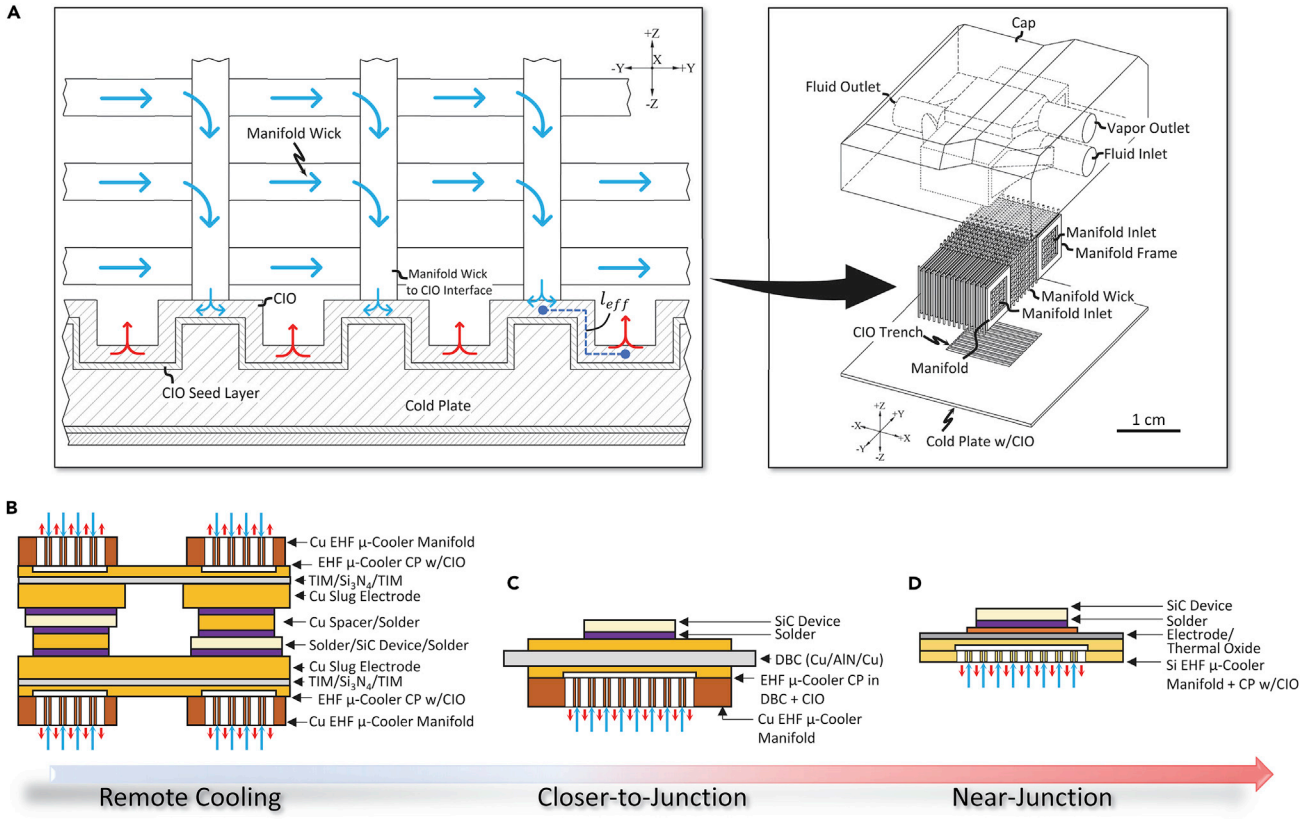


Figure 2. EHF μ-Cooler concept and package configurations

(A) EHF μ-Cooler concept for cooling of heat fluxes ~1 kW/cm^2 over large areas (1-3 cm^2); the left-side image (not shown to scale) illustrates a cut plane of the stacked Cu layer-based mesh manifold wick to cold plate CIO wick interface with CIO effective wicking length, l_{eff}; the right-side image provides an exploded perspective view of a full EHF μ-Cooler assembly including a cap structure.

(B–D) Remote cooling, (B), using an all-Cu EHF μ-Cooler that replaces a standard cold plate; electrical isolation is achieved using Si_3N_4 shims. Cooling closer to the junction, (C), with the EHF μ-Cooler CIO wick deposited on the bottom Cu layer of the package DBC; electrical isolation is achieved via the DBC AlN layer. Near-junction cooling, (D) by direct die attach of the semiconductor device to the EHF μ-Cooler; electrical isolation is achieved using a 1-2 μm thick thermal oxide layer across the entire top side of the cooling structure and under a Cu electrode. Note: blue arrows = cold single-phase liquid; red arrows = vapor.

power conversion application. The most aggressive near-junction cooling approach, Figure 2D, involves die attaching a Si wafer-based EHF μ-Cooler directly to the power semiconductor device. This assumes ~1 kV electrical isolation is provided by a 1-2 μm thick silicon oxide, SiO_2, layer with ~0.81 kV/μm dielectric strength[28,29] on top of the Si EHF μ-Cooler and below the lower Cu electrode of the power package. Additionally, a dielectric coolant, e.g., 3M Novec Engineered Fluid 649, 7100, 7500, for heat transfer may be employed with a typical dielectric strength of >9 kV/mm.

A consideration for increasing the power density of an electronics package is the ratio of the conductive thermal resistance of the package to the convective thermal resistance of the cooler. We initially assume deionized (DI) water as the coolant with an EHF μ-Cooler unit thermal resistance value[26] of $R''_{th\_c} \sim 0.012$ cm^2·°C/W over a 1 cm^2 actively cooled area, A_c, of the package. The conductive thermal resistance, R_{th_cnd}, of the power card structure shown in Figure 2B will dominate the total thermal resistance of the package,[30] i.e., $R_{tot} = R_{th\_cnd} + R''_{th\_c}/A_c \approx R_{th\_cnd}$ as $R_{th\_cnd} \gg R''_{th\_c}/A_c$. This conclusion is based on the large number of layers and thermal interfaces for the Figure 2B package. Thus, only the two DBC-based and direct-die-attach packages, Figures 2C and 2D, are retained for numerical modeling.

Thermal modeling and numerical results

Conduction-based finite element analysis in COMSOL Multiphysics® is used to model the two packages. The steady-state governing equation in a 3-D domain, Ω, assuming Einstein summation convention is,

Table 1. Coolant & wick properties for thermal analysis

Coolant	Saturation Temperature, T_{sat} [°C]	Superheat, ΔT [°C]	CHF,[26] q''_{CHF} [W/cm^2]	l_{eff} [μm]	R''_{th_c} [cm^2·°C/W]
DI Water	100	12	1000	218	0.012
HFO-1233zd	45	1.2	307	84	0.0039

$$Q = -\frac{\partial}{\partial x_i}\left(k_{ij}\frac{\partial T}{\partial x_j}\right) in\ \Omega, for\ i,j = 1,2,3, \quad \text{(Equation 1)}$$

where, T, is the temperature state variable, Q is the volumetric heat source, and k_{ij} are the thermal conductivity tensor components in a Cartesian coordinate system. Here, we neglect radiation heat transfer, and therefore the thermal boundary conditions (BCs) reduce to,

$$T_s = f(x,y,z)\ on\ \Gamma_T, and \quad \text{(Equation 2)}$$

$$-\left(k_{ij}\frac{\partial T}{\partial x_j}\right)n_i = q''_a + q''_{cnv}\ on\ \Gamma_{q''} \quad \text{(Equation 3)}$$

where a temperature BC is defined on boundary Γ_T, as $f(x,y,z)$ in Equation 2, and an applied heat flux, q''_a, is applied on boundary $\Gamma_{q''}$ in Equation 3 along with $q''_{cnv} = h(T - T_o)$, which is an applied convective flux that depends on the heat transfer coefficient, h, at a specified reference temperature, T_o.

In all models, an EHF μ-Cooler heat transfer coefficient is calculated based on the convective thermal resistance, $h = 1/R''_{th\_c}$, of the CIO for a selected working fluid; the reference temperature is taken as the sum of the fluid saturation temperature plus estimated superheat, $T_o = T_{sat} + \Delta T$, for a selected coolant. These values are provided in Table 1. Note that the coolant superheat is calculated by combining Kelvin and Clapeyron equations based on an approach in the literature.[31] Additionally, the applied heat flux in the numerical model is based on the critical heat flux (CHF) for the coolant, $q''_a = q''_{CHF}$, with details of CHF modeling also available in the literature.[26] Selected fluids include DI water[32] and HFO-1233zd,[33–35] the latter selected as a possible low temperature capable, very low global-warming potential coolant for harsh environment (e.g., vehicular) applications. Observe in Table 1 that a reduction in CHF is inevitable when adopting HFO-1233zd; however, R''_{th_c}, is very low leading to extremely high estimated heat transfer coefficients. Additionally, the CIO effective wicking length,[26] l_{eff}, in Table 1 (and shown in the illustration on the left in Figure 2A), is also affected by the selected coolant.

In the thermal model for the package, Figure 2C, a 1 cm^2 by 125 μm thick SiC device, k = 490 W/(m·K),[36] is assumed to be attached to a DBC substrate. The heat flux, q''_a, is applied to the top of the power device. Note that, in practical inverter applications, an array of smaller (e.g., ~0.25 cm^2) SiC devices may be used instead of a single large-area heat source. A high-temperature capable die-attach material like a transient liquid phase (TLP) bond[37] or a hybrid silver (Ag) particle paste attachment is considered. We select the Ag-based material with a 60 μm bond line thickness and a thermal conductivity of 74 W/(m·K).[38] The DBC in this package[39] is assumed to have Cu, k = 400 W/(m·K), layer thickness of 200 μm with an AlN, k = 170 W/(m·K), ceramic layer thickness of 630 μm. The cold plate area for the application of the heat transfer coefficient BC is positioned at the bottom of the DBC, where the lower Cu layer is assumed to be thinned to 100 μm for CIO deposition.

For the power semiconductor direct-die-attach case in Figure 2D, the same-size SiC device with identical heat flux is assumed to be directly attached to the Si, k = 150 W/(m·K), cold plate of the EHF μ-Cooler via a similar hybrid Ag bond, and the same heat transfer coefficient BC is applied. However, in this situation, an additional 1 μm SiO_2 thin layer with a thermal conductivity of 1.4 W/(m·K)[40] is utilized below the TLP bond/package electrode layer for ~0.81 kV[29] electrical isolation. This 1 μm SiO_2 layer thickness is deemed sufficient for a range of lower-power (e.g., solar energy harvesting or appliance) applications that often require less electrical isolation.[6] Another situation involving a 1.48 μm-thick SiO_2 layer is also explored for 1.2 kV electrical isolation, which is a common value for power conversion applications.[41] Figure 3 provides a detailed illustration of the one-quarter symmetry numerical model for this package configuration.

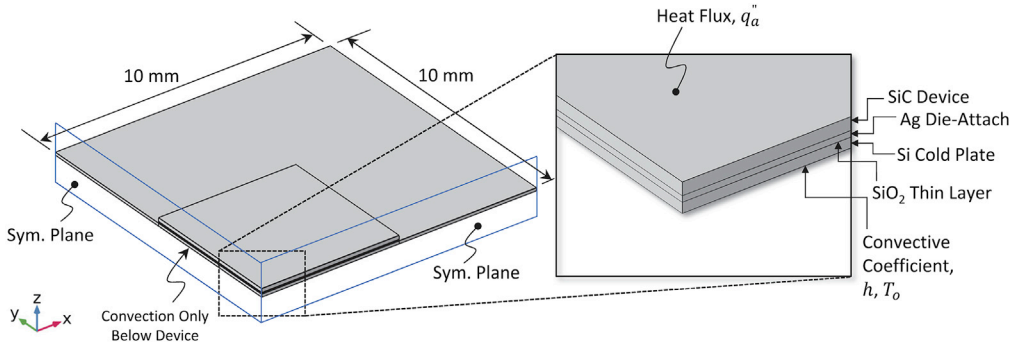


Figure 3. Model of EHF μ-Cooler direct-die-attached to power semiconductor

Representative one-quarter symmetry numerical model of EHF μ-Cooler Si cold plate direct-die-attached to a SiC device. The zoomed view on the right highlights the layers of the package including the SiO_2 thin thermal layer, applied loads, and convective heat transfer boundary condition, $h = 1/R''_{th\_c}$, for the EHF μ-Cooler.

The numerical results for the above packages are summarized in Table 2. The Configuration 1 power electronics package with an all-Cu EHF μ-Cooler having the CIO deposited directly on the bottom layer of the DBC (Figure 2C) has the highest estimated maximum device temperature of T_{max} = 177.7°C for q''_a = 1 kW/cm^2 with DI water as the coolant versus T_{max} = 63.9°C for q''_a = 0.307 kW/cm^2 with HFO-1233zd as the coolant. Moving closer to the junction, the Configuration 2B package with an all-Si EHF μ-Cooler direct-die-attached to the SiC device (Figure 2D) and with 1.48 μm of SiO_2 for 1.2 kV electrical isolation results in a significant 25.8°C and 7.9°C maximum temperature reduction when using DI water and HFO-1233zd, respectively. The best case, Configuration 2A (Figure 2D) with 1 μm of SiO_2, has estimated thermal performance that is very slightly better than that reported for Configuration 2B. Note that the junction-to-coolant unit thermal resistance for each package is also reported in Table 2, and Configuration 2A with HFO-1233zd as the coolant with R''_{th_jc} = 0.0284 cm^2·°C/W provides a 51% reduction in the unit thermal resistance relative to Configuration 1 with the same fluid. Observe that all package configurations lead to device temperatures well below a 200°C maximum junction temperature limit for SiC semiconductor devices.[41] The conclusion from this analysis of the closer-to-junction and near-junction packages is that the total unit thermal resistance results are approximately an order of magnitude lower than those reported in the literature for various commercial power electronics packages.[20]

Materials and methods

From the prior numerical analysis, we consider the near-junction EHF μ-Cooler assembly for the package that has the best thermal performance, Configuration 2A from Table 2. Thus, for the TEA we investigate the necessary materials and fabrication methods required for the development and low-volume (i.e., less than 200 parts per manufacturing run) production of the following: 1) an all-Si structure with a Si cold plate plus micro-fabricated Si manifold; 2) a hybrid structure with a Si cold plate plus a Cu-based layered mesh manifold. A description of each fabrication process flow is provided in combination with an explanation of the materials involved in each case.

For the case of an all-Si EHF μ-Cooler assembly, the base material inputs to the device fabrication include the materials for the Si cold plate plus the materials for the Si manifold. Both components utilize a 500-1000 μm thick Si wafer as a raw input. As shown in the upper branch of the flow diagram, Scheme 1, the fabrication process[42] for the cold plate includes steps for mask creation plus etching of fins and support structures for the CIO wick and the attachment of the manifold, respectively. This is followed by the deposition of metal on to the cold plate wafer for bonding to the manifold wafer. Likewise, the process for the manifold (middle branch of Scheme 1) involves steps where a mask is created to etch the fluid delivery channels into the wafer. Next, thermal oxide is re-grown on the manifold wafer as a new layer to improve smoothness of the bonding surfaces and as a stop layer for bonding. This is followed by the deposition of metal on to the wafer for the bonding of the manifold to the cold plate. Once these individual Si wafers are prepared, they are bonded as a precursor to the deposition of the polystyrene (PS) sphere template for CIO deposition. Three possible approaches to the PS sphere template deposition include sedimentation, drop casting, or application by doctor blade. Regardless of approach to the CIO PS sphere template

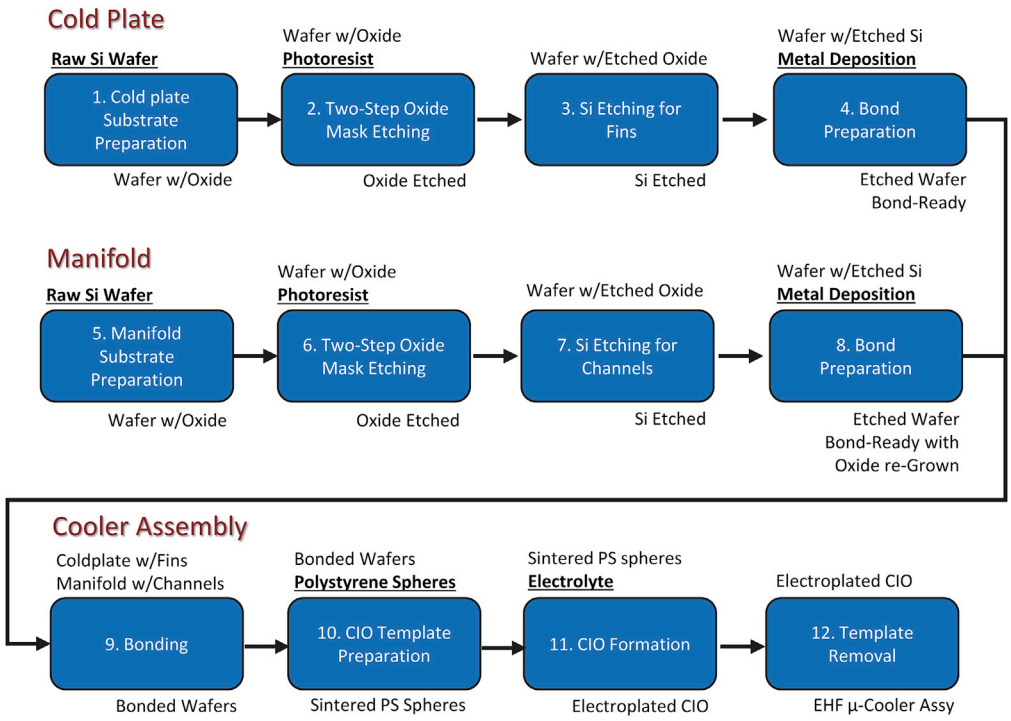
Table 2. Thermal model Configurations and numerical results for 1 cm² device

Configuration (Coolant)	Figure	Description	q''_a [W/cm²]	T_{max} [°C]	R''_{th_jc} [cm².°C/W]
1 (DI Water)	2C	Cu cooler in DBC substrate	1000	177.7	0.0657
1 (HFO-1233zd)	2C	Cu cooler in DBC substrate	307	63.9	0.0577
2A (DI Water)	2D	Si cooler direct die attached[a]	1000	148.5	0.0365
2A (HFO-1233zd)	2D	Si cooler direct die attached[a]	307	54.9	0.0284
2B (DI Water)	2D	Si cooler direct die attached[b]	1000	151.9	0.0399
2B (HFO-1233zd)	2D	Si cooler direct die attached[b]	307	56.0	0.0318

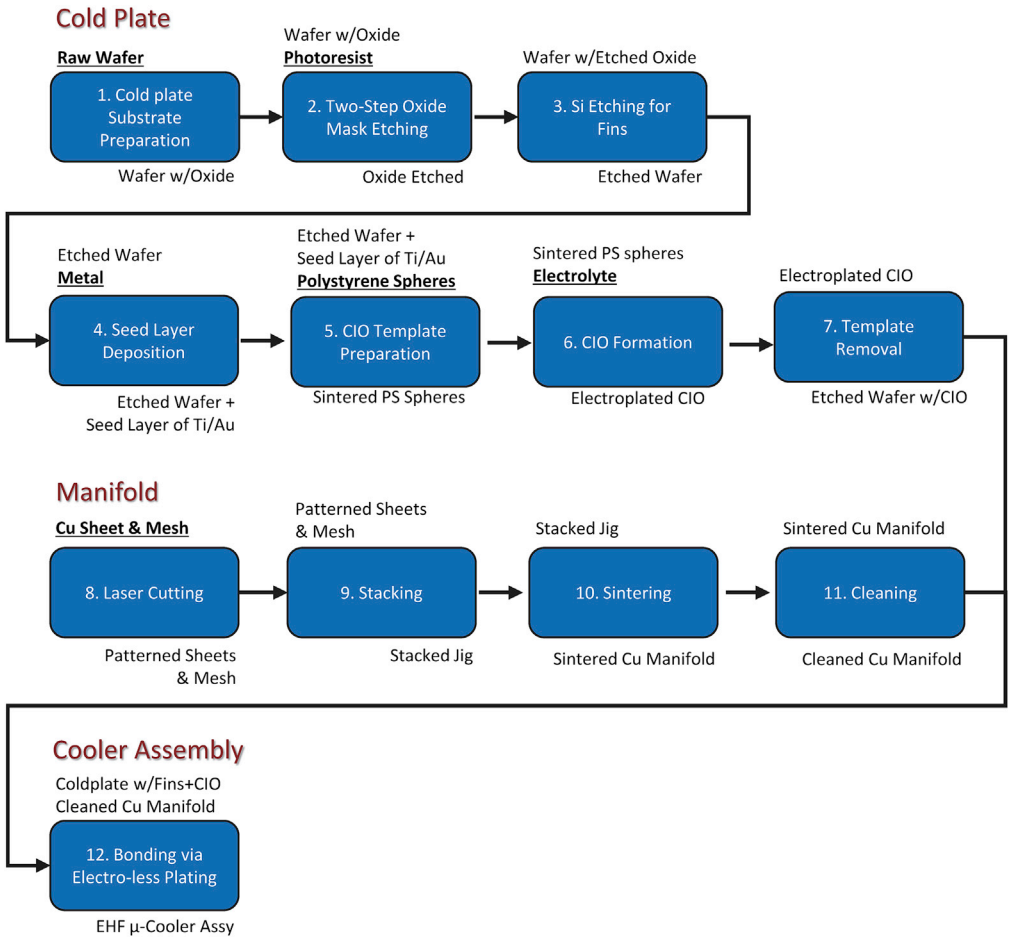
[a]SiO_2 thickness = 1 μm for ~0.81 kV electrical isolation.[29]
[b]SiO_2 thickness = 1.48 μm for ~1.2 kV electrical isolation.[29]

creation, after the deposition of the template, the PS spheres are sintered in preparation for electroplating the CIO structure. After electroplating, the PS sphere template is removed to reveal the Cu CIO wick, which results in the final all-Si EHF μ-Cooler assembly, Scheme 1 (lower branch).

The second process diagram for the fabrication of the hybrid EHF μ-Cooler assembly is shown in Scheme 2. We follow a similar approach to start with the fabrication of the Si cold plate, where we again utilize a 500 μm thick Si wafer as a raw input and then deposit a mask followed by the etching of the fins[42] and manifold support structures. To realize this cooler architecture, a titanium/gold (Ti/Au) metal seed layer for the CIO is further deposited on to the wafer before the deposition of the PS sphere template again using a sedimentation, drop casting, or doctor blade approach. After sintering the PS sphere template, the CIO structure is electroplated on the cold plate, and the PS sphere template is removed. Here, a metal layer is not applied for bonding the cold plate wafer to the manifold since an electro-less bonding method is tentatively proposed. Regarding the Cu manifold process flow in the middle branch of Scheme 2, raw material inputs to the start of the fabrication process include 50 μm to 250 μm thick Cu sheet and 50 × 50 to



Scheme 1. Fabrication of an All-Si EHF μ-Cooler
Process flow diagram for the fabrication of a chip-scale cooler assembly including a Si wafer-based cold plate mated to a Si wafer-based manifold for fluid delivery.



Scheme 2. Fabrication of a Hybrid EHF μ-Cooler

Process flow diagram for the fabrication of a hybrid cooler assembly including a Si wafer-based cold plate mated to a Cu-based layered mesh manifold for fluid delivery

600 × 600 mesh size (i.e., ~500 μm to ~50 μm opening size), 500 μm to 25 μm thick Cu mesh. Note that the thickness of the Cu sheet in the manifold relates to the wicking length, l_{eff} in Table 1 for the CIO cold plate, and dielectric liquids require finer features in the manifold and cold plate, so the wicking distance is shorter compared to that of water. Regardless, the Cu sheet and mesh is cut from bulk stock, cleaned, cut to size, and cleaned again before etching. The patterned Cu sheet and mesh is stacked in an assembly jig and sintered in a furnace. The final Cu manifold is then cleaned and etched once more. Lastly, an electro-less bonding approach is proposed to join the Si cold plate with CIO to the Cu manifold to arrive at the completed hybrid EHF μ-Cooler assembly.

Cost analysis

The process schemes for the fabrication of the two near-junction EHF μ-Cooler assembly architectures serve as a basis for economic analyses that were carried out by estimating associated production costs for each cooler configuration. The key parameters for material costs, fabrication costs, and operational costs, as inputs to the total production cost estimates, are listed in Table 3.

The total cost in U.S. dollars (USD) per all-Si EHF μ-Cooler is calculated as:

$$\frac{1}{N_w \times N_c} \times \left[\frac{1}{Y_{cr}} (SC + C_{TL_{cr}}) + \frac{1}{Y_{cio}} \left(\sum_{i=10}^{12} C_i + C_{TL_{cio}} \right) \right], with \quad \text{(Equation 4)}$$

Table 3. Variable and Fixed Process Costs as Inputs to the Total Production Cost of an EHF μ-Cooler Assembly for a 1 cm² Heat Source

All-Si EHF μ-Cooler Process (Scheme 1)			Hybrid EHF μ-Cooler Process (Scheme 2)		
Step	Item	Cost per Batch[a]	Step	Item	Cost per Batch[a]
1	Si Wafer[e] + Oxide Deposition	$260	1	Si Wafer[e] + Oxide Deposition	$260
2	Lithography + Oxide Etch	$1,140	2	Lithography + Oxide Etch	$1,140
3	Deep Si Etch + Wafer Cleaning	$500	3	Deep Si Etch + Wafer Cleaning	$500
4	Metal Deposition for Bonding	$325	4	E-beam Evaporation of Ti/Au	$220
5	Si Wafer[f] + Oxide Deposition	$260	5	PS Spheres + Template Formation[c] and Sintering	$240
6	Lithography + Oxide Etch	$1,140	6	CIO Formation	$480
7	Deep Si Etch + Wafer Cleaning	$1,450	7	PS Sphere Template Removal	$204
8	Grow/Deposit Oxide + Metal Deposition for Bonding	$825	8	Cu Sheets and Mesh[g] + Laser Cutting	$331
9	Wafer Alignment + Bonding	$3,600	9	Stacking of Patterned Cu Sheets and Mesh	$54[d]
10	PS Spheres + Template Formation[c] and Sintering	$240	10	Sintering of Cu Manifold	$60
11	CIO Formation	$480	11	Cleaning of Cu Manifold	$67
12	PS Sphere Template Removal	$204	12	Bond Manifold by Electro-less Plating	$240
–	Total Labor Costs for Clean Room Steps 1–9, $C_{TL_{cr}}$	$7,570[b]	–	Total Labor Costs for Clean Room Steps 1–4, $C_{TL_{cr}}$	$2,570[b]
–	Total Labor Costs for CIO Steps 10–12, $C_{TL_{cio}}$	$197[b]	–	Total Labor Costs for CIO Steps 5–7, $C_{TL_{cio}}$	$197[b]
–	–	–	–	Total Labor Costs for Manifold Steps 8–12, $C_{TL_{man}}$	$364[b]

[a]Assumes 1 batch = 8 wafers; 1 wafer = 15 parts.
[b]Assumes 1 employee with an average annual salary of $125,000.
[c]Assumes the drop casting method as preferred for template formation. PS sphere materials: Nonionic Latex Beads, 4% w/v, 5 μm; Electroplating solution: Copper(II) sulfate ACS reagent, = 98.0 7758-99-8 ; Acid: Sulfuric acid ACS reagent, 95.0-98.0 7664-93-9.
[d]Assumes a $450 jig per part is reusable 1,000 times.
[e]Si cold plate wafer: Alpha Nanotech Prime-Grade 4'' Silicon Wafers (P-Type, 525 um).
[f]Si manifold wafer: 1 mm thk, 4" Silicon Wafers, item F791.
[g]Cu manifold sheet (5 mil): 110 Copper Shim Rolls; Cu manifold mesh: Copper Wire Cloth.

$$SC = \$3,500 + \left(\sum_{i=1}^{9} C_i - \$3,500\right) \times 0.25. \qquad \text{(Equation 5)}$$

Here, N_w = 8 is the number of wafers per fabrication batch, N_c = 15 is the number of cooler parts per wafer, Y_{cr} = 0.9 is the assumed yield per batch (i.e., 90%) for the clean room fabrication process steps, and Y_{cio} = 0.75 is the assumed yield per batch (i.e., 75%) for the CIO fabrication process steps. In Equations 4 and 5, the process step costs, C_i, from Table 3 are summed over the number of i process steps. The term, $C_{TL_{cr}}$, in Equation 4 is the clean room total labor cost per batch from the second-to-last line in the first column of Table 3. Recall that the process steps for the micro-fabrication of the Si cold plate include steps 1-4, while steps 5-8 are for the Si manifold. The clean room total labor cost per batch, $C_{TL_{cr}}$, thus includes costs associated with all these steps. The CIO labor cost per batch is additionally $C_{TL_{cio}}$ in Equation 4 from the last line in the first column of the table. The term SC in Equation 4 and defined in Equation 5 is the nanofabrication facility graduated monthly fee formula that is applied to materials and tools used in the clean room based on a published Soft Cap rate of $3,500/month with a 75% discount on fees above this amount.[43]

Table 4. Near-junction cooling cost target and TEA metric results

Module device type[a]	Assumed efficiency[b]	Cooling technology	Cooling capacity [kW]	Cooler cost [$]	Module power [kW]	Cooler volume [mL]	*M1* [$/kW]	*M2* [kW/mL]
Si IGBT + Si Diode	98%	COTS mini-channel[44]	1[c]	300	50	525	6	0.095
SiC MOSFET	99%	COTS mini-channel[44]	1[c]	300	100	525	3	0.190
SiC MOSFET	99%	Hybrid EHF μ-Cooler	6[d]	594	600	40	0.99	15
SiC MOSFET	99%	Hybrid EHF μ-Cooler	1.84[e]	594	184	40	3.23	4.6

[a]Assumes a standard three-phase, full bridge, six-switch position inverter topology.[47,48]
[b]Based on results at the module level reported in the literature.[45,47,48]
[c]Glycol/water (30/70) coolant.[44]
[d]DI water coolant.
[e]HFO-1233zd coolant.

In the case of the hybrid EHF μ-Cooler assembly, the total cost in USD per cooler is calculated as:

$$\frac{1}{N_w \times N_c} \times \left[\frac{1}{Y_{cr}} \left(\sum_{i=1}^{4} C_i + C_{TL_{cr}} \right) + \frac{1}{Y_{cio}} \left(\sum_{i=5}^{7} C_i + C_{TL_{cio}} \right) + \frac{1}{Y_{man}} \left(\sum_{i=8}^{12} C_i + C_{TL_{man}} \right) \right] \quad \text{(Equation 6)}$$

The additional terms, Y_{man} and $C_{TL_{man}}$, in Equation 6 are the assumed yield for the manifold fabrication steps (i.e., 95%) and the manifold labor cost per batch, respectively. We assume the Cu sheet metal and mesh cutting plus subsequent stacking processes, steps 8-11 in the second column of Table 3 are highly scalable to very large volumes in the future using automated sheet metal stamping and stacking techniques and equipment. Note that we do not include the amortized cost of such capital purchases for extremely large-scale production in this TEA.

Cost target for near-junction cooling

For near-junction cooling to be cost competitive and widely adopted across a range of energy-related WBG power electronics applications, the technology must provide a robust thermal management solution at a very low price point. Here, we consider the cost of the cooling technology per kilowatt, $/kW, at a power electronics module system level to connect to the impact of higher efficiency WBG device adoption in combination with high-performance cooling. A standard commercial-off-the-shelf (COTS) single-phase (i.e., liquid cooled) mini-channel cooler[44] with a total cooling capacity of 1 kW, cost of ~$300, and volume of ~525 mL is selected as a representative reference technology, although other similar COTS products could be selected. We further assume 98% efficiency for a Si device power module versus 99% efficiency for a SiC WBG power module.[45] Thus, the maximum module power level that might be cooled by the reference cooling technology is 50 kW and 100 kW for the Si and SiC cases, respectively. Note that the ability to significantly increase the system power for the same switching frequency due to reduced semiconductor losses when moving to WBG devices is verified experimentally in the literature.[45,46] Assuming a 6-in-1 (i.e., standard three-phase, full bridge, six-switch position) inverter topology[47,48] is accommodated by the reference cooler, we calculate a benchmark cooling cost per kilowatt metric,

$$M1 = Cooler\ Cost / Module\ Power \quad \text{(Equation 7)}$$

of $6/kW for the cooling of a Si power electronics module versus $3/kW for cooling a SiC module. Additionally, the volumetric power density metric for the cooler in a Si and SiC power module assembly,

$$M2 = Module\ Power / Cooler\ Volume \quad \text{(Equation 8)}$$

is 0.095 kW/mL and 0.190 kW/mL, respectively. The reader is referred to Table 4 for a summary of the cost targets.

Techno-economic analysis results

With the variable and fixed process cost values listed in Table 3 of the prior section inputted to Equations 4 and 5, we obtain a total cost per all-Si EHF μ-Cooler of $129, where primary costs associated with materials, processes, and labor are incurred in the clean room during the microfabrication of the Si cold plate and manifold wafers. Based on the first column in Table 3, the wafer alignment and bonding process is a particularly large cost driver. Regarding the hybrid EHF μ-Cooler assembly, we obtain a total cost per cooler of $66 using Equation 6 and this cost is approximately half of that of the all-Si version cooler.

Considering either near-junction cooled package from Table 2 and again a 6-in-1 SiC WBG inverter power module, the EHF μ-Cooler technology can handle up to 1 kW or 0.307 kW of power (over >1 cm^2 footprint area) per switch position for packages with DI water or HFO-1233zd coolant, respectively. Thus, a six-switch position SiC power module at 99% efficiency could theoretically reach a power level of 600 kW or 184 kW, respectively, if cooled with DI water or HFO-1233zd. This module-level cooler is estimated to be 40 mL (i.e., 5 cm x 4 cm x 2 cm) in size with a cost of ~$594 corresponding to six 1.23 × 1.23 cm^2 individual hybrid EHF μ-Coolers; note that we slightly scale up the footprint area and cost of each individual cooler to account for common module-level packaging considerations such as the spacing of multiple power devices per switch position.[48] Thus, we obtain the product metrics $M1 \approx 0.99$ $/kW and $M2 \approx 15$ kW/mL using DI water as the coolant or $M1 \approx 3.23$ $/kW and $M2 \approx 4.6$ kW/mL with HFO-1233zd as the coolant. These results are summarized in Table 4.

Depending on the selected cooling fluid, the results in Table 4 stemming from the TEA represent an approximate 75× to 25× improvement in the volumetric power density of the cooler for one-third to roughly equal cost per kW of module power. Another perspective on this result through the lens of adopting WBG devices with high-performance cooling clearly relates to the ability to push a power module to even higher switching frequencies (e.g., upwards of 200 kHz).[45] This is associated with further increases in volumetric/gravimetric power density due power module passive size reduction (e.g., above 70%)[45,47] and end application efficiency improvements (e.g., 5-10% fuel efficiency savings at the vehicle level).[46]

DISCUSSION

System-level implementation considerations

For high-power-density power electronics, an associated coolant flow loop found in a harsh-environment application typically utilizes single-phase 50/50 mixture by volume of water/ethylene-glycol. Such binary fluids may have additional additives that have unknown (and possibly detrimental) effects on boiling heat transfer.[49] These binary coolants are further considered inadequate for two-phase heat transfer due to the different liquid-to-vapor phase transition temperatures of the constitutive fluids which suppresses the onset of boiling relative to water and presents additional thermal resistance.[50,51] A conventional liquid flow loop in a harsh environment that has an electric machine connected in series with the power electronics should be modified to isolate any two-phase power electronics cooling loop from the existing system single-phase cooling loop to enable the use of alternative fluids and possibly higher system pressures.[49] A liquid-to-liquid heat exchanger (HX) to exchange energy extracted from the secondary two-phase loop and pass it to the primary single-phase loop might be employed to achieve this isolation, and examples of such systems are found in data centers.[52] While the specific design details and attendant cost ramifications of this secondary flow loop are application dependent and thus beyond the scope this TEA, such system-level considerations are worth identifying.

A cooling system that employs two-phase heat transfer also may be subject to pressure and temperature fluctuations associated with liquid-vapor flow instabilities. These have been the subject of extensive study.[19,53,54] Particularly, for flow boiling in channels, liquid and vapor phase density differences generate a range of effects that can lead to increasing channel pressure drop with decreasing flow and attendant instability. The key aspect leading to instability is the interaction of the liquid and vapor flow. Since the EHF μ-Cooler assembly is expected to produce high vapor exit qualities in a capillary-fed configuration, the concept aims to minimize pressure instabilities and orientation effects by effectively separating the liquid flow to the boiling surface at the wick and vapor flow away from it.[55] The implementation of a hybrid EHF μ-Cooler assembly with a Cu-based manifold is expected to further benefit temperature instabilities through added thermal capacitance plus well-directed and large vapor outflow paths. These two-phase flow and heat transfer effects should be confirmed at the system-level for given applications.

Market recommendations

Compared with COTS cooling solutions for power electronics, the estimated cooling cost per kilowatt of module power for the hybrid EHF μ-Cooler manufactured for low-volume (i.e., less than 200 parts) production is likely cost competitive in the marketplace. However, further process refinements and improvements are recommended to increase the yield for the clean room, CIO, and Cu manifold fabrication steps. Additional cost reduction efforts for the all-Si EHF μ-Cooler should focus on the highest cost items associated with the clean room fabrication process identified in Table 3. Leveraging process innovations,[42] it is conceivable that fabrication steps may be reduced to the processing of a single wafter for the all-Si EHF μ-Cooler configuration which would positively reduce costs associated with material and labor. Beyond such improvements, and building off this TEA, EHF μ-Cooler configurations built from other substrate

systems, such as DBC substrates,[20] aluminum (Al), or AlSiC metal matrix composites,[56] might also be considered as part of next-step cost/weight reduction or performance metric improvement efforts. For example, the use of a DBC substrate may offset a significant portion of the most expensive (i.e., Si microfabrication) steps of the current EHF μ-Cooler fabrication schemes.

Based on industry discussions, multi-chip package (MCP) applications are of interest where cooling can be adaptively delivered to the hottest spot over an array of chips. For future power electronics, since individual WBG chip size is decreasing with the adoption of new materials such as SiC, customizing a cooler for an array of devices (e.g., multiple devices per switch position) may be a key point. Advantageously, the CIO architecture of the EHF μ-Cooler further enables customization since both the manifold and CIO may be structurally/modularly designed or functionally graded in-plane for preferred fluid delivery pathways. While the numerical modeling in this TEA showed that the EHF μ-Cooler can control power semiconductor device to ~175°C for a 1 kW/cm^2 heat flux, the appropriateness of this uniformly applied 1 kW/cm^2 heat flux ultimately depends on a specific power electronics circuit or MCP architecture and particular industry partner requirements. Accordingly, scalability of the cooler architecture and fabrication processes is further identified as an important aspect for future market consideration along with functional testing of power devices once the cooler is integrated into the package.

Conclusions

In this perspective, a TEA was presented for a near-junction extreme-heat-flux micro-cooler for high-performance thermal management of WBG power electronics based on a high-level view of the energy impact of such power conversion systems. A brief review of the relevant literature was provided to summarize feasible integration approaches for near-junction cooling in power electronics. The EHF μ-Cooler concept was then introduced, and candidate packages were proposed. Note that the TEA is mainly dependent on these packages and associated integration approaches. Numerical analysis of the thermal performance of these packages then allowed for the identification of promising configurations with the cooler incorporated into either a DBC substrate or direct die attached to the power device. Two near-junction EHF μ-Cooler architectures were then described including an all-Si structure and a hybrid structure with Si cold plate plus Cu manifold. The materials and manufacturing processes required for the fabrication of each type of cooler were provided along with estimates of labor costs to arrive at low-volume production cost estimates for each cooler. Market recommendations and directions for future work to move the technology toward industry adoption were provided. Important ongoing work includes prototype fabrication and associated performance plus reliability testing.

Limitations of the study

A primary limitation of the present study relates to uncertainty in the cost analysis due to economies of scale. Here, we use academic rates in the cleanroom microfabrication portion of the cost analysis. However, on the opposite side of the argument, we are considering small-batch pricing from a university, whereas the COTS cold plate system presumably is based on larger-scale production with better economies of scale. Fully capturing these inter-relationships without scaling up production either at an in-house facility or at an outside foundry is a limitation of this study. The same economies of scale are relevant when we discuss labor benefits and overhead costs, which depend heavily on the skill level of the labor employed, number of employees required for mass production, employment region, and company or service.

Additional practical considerations that are currently under investigation relate to the reliability testing of both the CIO in terms of boiling erosion and corrosion and the full EHF μ-Cooler in terms of thermal cycling. The evaluation of the selected coolant for harsh-environment application and its impact on the EHF μ-Cooler thermal performance is another aspect to study. Other relevant investigations may examine thermal-mechanical issues related to the attachment of the EHF μ-Cooler to a package or within the cooler itself, although such integration issues may again be more suited to follow-on commercialization efforts for a specific chosen application. Likewise, verification of pumping power benefits for this type of capillary-based cooler is ongoing; however, system pumping power evaluation is heavily dependent on the final cooling fluid loop implementation for a particular application.

Finally, challenges to commercialization and production scale-up for microfabrication-related technologies can be formidable, as illustrated by microelectromechanical systems (MEMS) historical perspectives.[57] However, for

the EHF μ-Cooler, the concept may not involve as many challenges associated with niche markets, multidomain optimization, and very large-scale integration. Thus, we hold the MEMS industry as a point of reference, and we identify that our challenges are different and perhaps not as severe in terms of scaling up. Whether the EHF μ-Cooler becomes the preferred solution for cooling of high-heat-flux electronics is indeed an area of uncertainty given efforts from multiple research groups. Nonetheless, this TEA serves as a starting point to identify pain points for further innovation to bring related near-junction cooling concepts to fruition in broad energy-related markets.

STAR★METHODS

Detailed methods are provided in the online version of this paper and include the following:

- KEY RESOURCES TABLE
- RESOURCE AVAILABILITY
  - Lead contact
  - Material availability
  - Data and code availability
- EXPERIMENTAL MODEL AND SUBJECT DETAILS
- METHOD DETAILS
  - CIO preparation
  - Si manifold preparation
  - Cu manifold preparation
- QUANTIFICATION AND STATISTICAL ANALYSIS

ACKNOWLEDGMENTS

Data contained herein was generated under a project that was funded, in part, by the Advanced Research Projects Agency-Energy (ARPA-E), an agency of the United States Government, U.S. Department of Energy, under Award Number DE-AR0001055 in the OPEN program monitored by Dr. Peter de Bock.

This work was co-authored in part by the National Renewable Energy Laboratory, operated by Alliance for Sustainable Energy, LLC, for the U.S. Department of Energy (DOE) under Contract No. DE-AC36-08GO28308. Funding was provided by ARPA-E. The views expressed in the article do not necessarily represent the views of the DOE or the U.S. Government. The U.S. Government retains and the publisher, by accepting the article for publication, acknowledges that the U.S. Government retains a nonexclusive, paid-up, irrevocable, worldwide license to publish or reproduce the published form of this work, or allow others to do so, for U.S. Government purposes.

AUTHOR CONTRIBUTIONS

Conceptualization, M.A., K.E.G., J.P., C.Z., Q.W., S.R., M.S., N.S., R.G., S.H., and E.D.; methodology, E.D., M.A., J.P., M.S., Q.W., S.H., C.Z., S.N., and B.K.; investigation, E.D., C.Z., Q.W., S.H., J.P., M.S., and R.G.; formal analysis, E.D., C.Z., M.A., and S.N.; visualization, E.D. and C.Z.; writing – original draft, E.D.; writing – review and editing, E.D., S.N., M.A., and C.Z.; supervision, M.A. and K.E.G.; project administration, K.E.G., M.A., J.P., S.N., and E.D.; funding acquisition, K.E.G., M.A., J.P., S.N., and E.D.

DECLARATION OF INTERESTS

E.D. has patent pending to Toyota Motor Engineering & Manufacturing North America, Inc. S.H., C.Z., Q.W., M.A., and K.E.G. have patent pending to The Board of Trustees of the Leland Stanford Junior University. M.S., N.S., S.R., R.G., and J.P. have patent pending to The Regents of the University of California (Merced). B.K. and S.N. have patent pending to Alliance for Sustainable Energy, LLC.

INCLUSION AND DIVERSITY

We support inclusive, diverse, and equitable conduct of research.

Received: July 28, 2022
Revised: November 1, 2022
Accepted: December 9, 2022
Published: January 20, 2023

REFERENCES

1. Tolbert, L.M., King, T.J., Ozpineci, B., Campbell, J.B., Muralidharan, G., Rizy, D.T., Sabau, A.S., Zhang, H., Zhang, W., Xu, Y., et al. (2005). Power Electronics for Distributed Energy Systems and Transmission and Distribution Applications. Oak Ridge National Laboratory Report No. ORNL/TM-2005/230. https://info.ornl.gov/sites/publications/Files/Pub57485.pdf.

2. Bose, B.K. (2013). Global energy scenario and impact of power electronics in 21st century. IEEE Trans. Ind. Electron. *60*, 2638–2651.

3. U.S. Department of Energy (2015). Quadrennial Technology Review – an Assessment of Energy Technologies and Research Opportunities. https://www.energy.gov/sites/prod/files/2017/03/f34/quadrennial-technology-review-2015_1.pdf.

4. Kizilyalli, I.C., Carlson, E.P., Cunningham, D.W., Manser, J.S., Xu, Y., and Liu, A.Y. (2018). Wide Band-Gap Semiconductor Based Power Electronics for Energy Efficiency. United States Department of Energy Report, ARPA-e. https://arpa-e.energy.gov/sites/default/files/documents/files/ARPA-E_Power_Electronics_Paper-April2018.pdf.

5. Gao, Y., Sankaranarayanan, V., Dede, E.M., Ghosh, A., Maksimovic, D., and Erickson, R.W. (2019). Drive-cycle optimized 99% efficient SiC boost converter using planar inductor with enhanced thermal management. In 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), pp. 1–7.

6. Lei, Y., Barth, C., Qin, S., Liu, W.-C., Moon, I., Stillwell, A., Chou, D., Foulkes, T., Ye, Z., Liao, Z., et al. (2016). A 2 kW, single-phase, 7-level, GaN inverter with an active energy buffer achieving 216 W/in3 power density and 97.6% peak efficiency. In 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 1512–1519.

7. Hamada, K., Nagao, M., Ajioka, M., and Kawai, F. (2015). SiC – emerging power device technology for next-generation electrically powered environmentally friendly vehicles. IEEE Trans. Electron. Dev. *62*, 278–285.

8. Saidur, R., Mekhilef, S., Ali, M.B., Safari, A., and Mohammed, H.A. (2012). Applications of variable speed drive (VSD) in electrical motors energy savings. Renew. Sustain. Energy Rev. *16*, 543–550.

9. Wheeler, P., and Bozhko, S. (2014). The more electric aircraft: technology and challenges. IEEE Electrific. Mag. *2*, 6–12.

10. Warren, J.A., Riddle, M.E., Graziano, D.J., Das, S., Upadhyayula, V.K.K., Masanet, E., and Cresko, J. (2015). Energy impacts of wide band gap semiconductors in U.S. light-duty electric vehicle fleet. Environ. Sci. Technol. *49*, 10294–10302.

11. Narumanchi, S., Mihalic, M., Moreno, G., and Bennion, K. (2012). Design of light-weight, single-phase liquid-cooled heat exchanger for automotive power electronics. In 13th InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM), pp. 693–699.

12. Dede, E.M. (2014). Single-phase microchannel cold plate for hybrid vehicle electronics. In 2014 Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM), pp. 118–124.

13. Bar-Cohen, A. (2013). Gen-3 thermal management technology: role of microchannels and nanostructures in an embedded cooling paradigm. J. Nanotechnol. Eng. Med. *4*, 020907.

14. Jankowski, N.R., Everhart, L., Geil, B.R., Tipton, C.W., Chaney, J., Heil, T., and Zimbeck, W. (2008). Stereolithographically fabricated aluminum nitride microchannel substrates for integrated power electronics cooling. In 11th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM), pp. 180–188.

15. Harpole, G.M., and Eninger, J.E. (1991). Microchannel heat exchanger optimization. In 7th IEEE Semi-Therm Symposium (SEMI-THERM), pp. 59–63.

16. Sharar, D.J., Jankowski, N.R., and Morgan, B. (2010). Thermal performance of a direct-bond-copper aluminum nitride manifold-microchannel cooler. In 2010 IEEE Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM), pp. 68–73.

17. Lee, H., Smet, V., and Tummala, R. (2020). A review of SiC power module packaging technologies: challenges, advances, and emerging Issues. IEEE J. Emerg. Sel. Topics Power Electron. *8*, 239–255.

18. Vladimirova, K., Crebier, J.-C., Avenas, Y., and Schaeffer, C. (2013). Drift region integrated microchannels for direct cooling of power electronic devices: advantages and limitations. IEEE Trans. Power Electron. *28*, 2576–2586.

19. Mudawar, I. (2001). Assessment of high-heat-flux thermal management schemes. IEEE Trans. Compon. Packag. Technol. *24*, 122–141.

20. Moreno, G., Narumanchi, S., Feng, X., Anschel, P., Myers, S., and Keller, P. (2021). Electric-drive vehicle power electronics thermal management: current status, challenges, and future directions. J. Electron. Packag. *144*, 011004.

21. Zhou, F., Joshi, S.N., Liu, Y., and Dede, E.M. (2019). Near-junction cooling for next-generation power electronics. Int. Commun. Heat Mass Tran. *108*, 104300.

22. Jung, K.W., Kharangate, C.R., Lee, H., Palko, J., Zhou, F., Asheghi, M., Dede, E.M., and Goodson, K.E. (2019). Embedded cooling with 3D manifold for vehicle power electronics application: single-phase thermal-fluid performance. Int. J. Heat Mass Tran. *130*, 1108–1119.

23. Reilly, S.W., and Catton, I. (2009). Improving biporous heat transfer by addition of monoprous interface layer. In ASME 2009 Heat Transfer Summer Conference, pp. 327–333.

24. Sudhakar, S., Weibel, J.A., Zhou, F., Dede, E.M., and Garimella, S.V. (2019). Area-scalable high-heat-flux dissipation at low thermal resistance using a capillary-fed two-layer evaporator wick. Int. J. Heat Mass Tran. *135*, 1346–1356.

25. Shaeri, M.R., Bonner, R.W., and Ellis, M.C. (2020). Thin hybrid capillary two-phase cooling system. Int. Commun. Heat Mass Tran. *112*, 104490.

26. Zhang, C., Palko, J.W., Barako, M.T., Asheghi, M., and Goodson, K.E. (2021). Design and optimization of well-ordered microporous copper structure for high heat flux cooling applications. Int. J. Heat Mass Tran. *173*, 121241.

27. Broughton, J., Smet, V., Tummala, R.R., and Joshi, Y.K. (2018). Review of thermal packaging technologies for automotive power electronics for traction purposes. J. Electron. Packag. *140*, 040801.

28. Yamabe, K., Taniguchi, K., and Matsushita, Y. (1983). Thickness dependence of dielectric breakdown failure of thermal SiO_2 films. In 21st International Reliability Physics Symposium, pp. 184–190.

29. Bartzsch, H., Glöß, D., Frach, P., Gittner, M., Schultheiß, E., Brode, W., and Hartung, J. (2009). Electrical insulation properties of sputter-deposited SiO_2, Si_3N_4 and Al_2O_3 films at room temperature and 400 °C. Phys. Stat. Sol. *206*, 514–519.

30. Incropera, F.P. (1999). Liquid Cooling of Electronics Devices by Single-phase Convection (John Wiley & Sons).

31. Ćoso, D., Srinivasan, V., Lu, M.C., Chang, J.Y., and Majumdar, A. (2012). Enhanced heat transfer in biporous wicks in the thin liquid film evaporation and boiling regimes. J. Heat Tran. *134*, 101501.

32. Lemmon, E.W., Huber, M.L., and McLinden, M.O. (2018). NIST Standard Reference Database 23. Reference Fluid Thermodynamic and Transport Properties (REFPROP), version 9.1.

33. Miyara, A., Alam, M.J., and Kariya, K. (2018). Measurement of viscosity of trans-1-chloro-3, 3, 3-trifluoropropene (R-1233zd(E)) by tandem capillary tubes method. Int. J. Refrig. *92*, 86–93.

34. Hulse, R.J., Basu, R.S., Singh, R.R., and Thomas, R.H.P. (2012). Physical properties of HCFO-1233zd(E). J. Chem. Eng. Data *57*, 3581–3586.

35. Thermodynamic Properties of HFO-1233zd. https://nl.climalife.dehon.com/uploads/product/media/document/hfo-r-1233zd-en.pdf.

36. Weitzel, C.E., Palmour, J.W., Carter, C.H., Moore, K., Nordquist, K.K., Allen, S., Thero, C., and Bhatnagar, M. (1996). Silicon carbide

high-power devices. IEEE Trans. Electron. Dev. *43*, 1732–1741.

37. Liu, Y., Joshi, S.N., and Dede, E.M. (2020). Novel transient liquid phase bonding for high-temperature automotive power electronics systems. J. Electron. Packag. *142*, 011003.

38. Suganuma, K., Sakamoto, S., Kagami, N., Wakuda, D., Kim, K.-S., and Nogi, M. (2012). Low-temperature low-pressure die attach with hybrid silver particle paste. Microelectron. Reliab. *52*, 375–380.

39. Rogers, C. (2021). curamik® ceramic substrates technical data sheet. https://rogerscorp.com/-/media/project/rogerscorp/documents/advanced-electronics-solutions/english/product-information/curamik-ceramic-substrates-product-information-and-data-sheet.pdf.

40. MKS (2022). Dielectric Thin Films. https://www.mksinst.com/n/dielectric-thin-films.

41. Chen, Z., Yao, Y., Boroyevich, D., Ngo, K.D.T., Mattavelli, P., and Rajashekara, K. (2014). A 1200-V, 60-A SiC MOSFET multichip phase-leg module for high-temperature, high-frequency applications. IEEE Trans. Power Electron. *29*, 2307–2320.

42. Hazra, S., Zhang, C., Wu, Q., Asheghi, M., Goodson, K., Dede, E.M., Palko, J., and Narumanchi, S. (2022). A novel hardmask-to-substrate pattern transfer method for creating 3D, multi-level, hierarchical, high aspect-ratio structures for applications in microfluidics and cooling technologies. Sci. Rep. *12*, 12180.

43. Stanford Nanofabrication Facility (2021). FY21 Equipment and Staff Fees. https://snfexfab.stanford.edu/docs/equipment-use-fees/fy21-equipment-and-staff-fees.

44. ATS-CP Series Liquid Cold Plates. https://www.digikey.com/en/product-highlight/a/advanced-thermal-solutions/ats-cp-series-liquid-cold-plates.

45. Han, D., Noppakunkajorn, J., and Sarlioglu, B. (2014). Comprehensive efficiency, weight, and volume comparison of SiC- and Si-based bidirectional DC–DC converters for hybrid electric vehicles. IEEE Trans. Veh. Technol. *63*, 3001–3010.

46. Ogawa, T., Tanida, A., Yamakawa, T., and Okamura, M. (2016). Verification of fuel efficiency improvement by application of highly effective silicon carbide power semiconductor to HV inverter. In SAE Technical Paper 2016-01-1230.

47. Ishino, H., Watanabe, T., Sugiura, K., and Tsuruta, K. (2014). 6-in-1 silicon carbide power module for high performance of power electronics systems. In IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD), pp. 446–449.

48. Shirabe, K., Swamy, M., Kang, J.-K., Hisatsune, M., Das, M., Callanan, R., and Lin, H. (2013). Design of 400V class inverter drive using SiC 6-in-1 power module. In 2013 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 2363–2370.

49. Sharar, D., Jankowski, N.R., and Morgan, B. (2010). Review of Two-phase Electronics Cooling for Army Vehicle Applications (Army Research Laboratory). Technical Report ARL-TR-5323.

50. Kandlikar, S.G., and Bulut, M. (2003). An experimental investigation on flow boiling of ethylene-glycol/water mixtures. J. Heat Tran. *125*, 317–325.

51. Moreno, G., Oldenburg, S.J., You, S.M., and Kim, J.H. (2005). Pool boiling heat transfer of alumina-water, zinc oxide-water and alumina-water+ethylene glycol nanofluids. In Heat Transfer Summer Conference, pp. 625–632.

52. ASHRAE (2019). Water-Cooled Servers: Common Designs, Components, and Processes (The American Society of Heating, Refrigerating and Air-Conditioning Engineers). https://www.ashrae.org/File%20Library/Technical%20Resources/Bookstore/WhitePaper_TC099-WaterCooledServers.pdf.

53. Ruspini, L.C., Marcel, C.P., and Clausse, A. (2014). Two-phase flow instabilities: a review. Int. J. Heat Mass Tran. *71*, 521–548.

54. Tadrist, L. (2007). Review on two-phase flow instabilities in narrow spaces. Int. J. Heat Fluid Flow *28*, 54–62.

55. Palko, J.W., Lee, H., Zhang, C., Dusseault, T.J., Maitra, T., Won, Y., Agonafer, D.D., Moss, J., Houshmand, F., Rong, G., et al. (2017). Extreme two-phase cooling from laser-etched diamond and conformal, template-fabricated microporous copper. Adv. Funct. Mater. *27*, 1703265.

56. Pahinkar, D.G., Puckett, W., Graham, S., Boteler, L., Ibitayo, D., Narumanchi, S., Paret, P., DeVoto, D., and Major, J. (2018). Transient liquid phase bonding of AlN to AlSiC for durable power electronic Packages. Adv. Eng. Mater. *20*, 1800039.

57. Peeters, E. (1997). Challenges in commercializing MEMS. IEEE Comput. Sci. Eng. *4*, 44–48.

STAR★METHODS

KEY RESOURCES TABLE

REAGENT or RESOURCE	SOURCE	IDENTIFIER
Chemicals, peptides, and recombinant proteins		
CIO electroplating solution: Copper(II) sulfate ACS reagent, = 98.0 7758-99-8	Sigma-Aldrich Solutions	Cat#209198
CIO acid: Sulfuric acid ACS reagent, 95.0–98.0 7664-93-9	Sigma-Aldrich Solutions	Cat#258105
Dissolving PS spheres: Tetrahydrofuran	Thermo Fisher Scientific	Cat#T397-500
Cu manifold clean: Sodium hydroxide (NaOH)	Sigma-Aldrich Solutions	Cat#1.06498
Cu manifold etch: Sulfuric acid 50% (H_2SO_4)	VWR International, LLC	Cat#BDH7371-2
Software and algorithms		
Thermal modeling: COMSOL Multiphysics® 5.6	COMSOL	https://www.comsol.com/
Si manifold exposure sketches: CleWin 4.0	Informer Technologies, Inc.	https://clewin.software.informer.com/
Cu manifold jig design: SolidWorks®	Dassault Systèmes SolidWorks Corporation	https://www.solidworks.com/
Other		
PS sphere materials: Nonionic Latex Beads, 4% w/v, 5 μm	Thermo Fisher Scientific	Cat#N37460
Si cold plate wafer: Alpha Nanotech Prime-Grade 4'' Silicon Wafers (P-Type, 525 μm)	Amazon	https://www.amazon.com/dp/B07JZV8BDL?th=1
Si manifold wafer: 1 mm thk, 4" Silicon Wafers	EL-CAT, Inc.	Cat#F791
Cu manifold sheet: 110 Copper Shim Rolls (5 mil)	Trinity Brand Industries	https://products.trinitybrand.com/viewitems/copper/110-copper-shim-rolls
Cu manifold mesh: Copper Wire Cloth	McMaster-Carr	https://www.mcmaster.com/wire-mesh/copper-wire-cloth/mesh-size~100-100/

RESOURCE AVAILABILITY

Lead contact

Further information and requests for resources relevant to this work should be directed to and will be fulfilled by the lead contact, Ercan M. Dede (eric.dede@toyota.com).

Material availability

This study did not generate new unique reagents.

Data and code availability

The data reported in this paper are available from the lead contact upon reasonable request.

This paper does not report original code.

Any additional information required to reanalyze the data reported in this paper is available from the lead contact upon reasonable request.

EXPERIMENTAL MODEL AND SUBJECT DETAILS

This study does not use experimental methods typical in the life sciences.

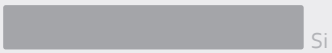
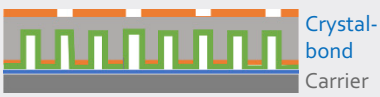
METHOD DETAILS

CIO preparation

For both all-Si and hybrid EHF μ-Coolers, the CIO is deposited by template-assisted electrodeposition. First, the target deposition surface is cleaned in acetone, isopropanol, and water, and soaked in piranha solution (sulfuric acid and hydrogen peroxide 9:1 mixture) for 15 minutes. Then, thoroughly mixed and sonicated 4% polystyrene (PS) spheres colloid (Sigma-Aldrich) is pipetted into the target area of the surface. The sample is left in open air at a 15 degree tilted angle until the solvent (DI water) fully evaporates, where the PS spheres are sedimented into close packing. The sedimented PS spheres are then sintered in a dry heater bath (Corning) at 107 °C for 60 minutes. After sintering, the sample is put into an electrolyte solution (0.6 M copper(II) sulfate, and 0.5 mM sulfuric acid) carefully after pre-wetting with ethanol, where copper is electroplated into the interstices of the PS template with a constant current deposition at 5–10 mA/cm^2. Lastly, the chip is submerged in tetrahydrofuran (Fisher Scientific) solution for 1–2 days until the PS templates are fully dissolved, and the CIO structure is revealed.

Si manifold preparation

For the all-Si μ-Cooler, the Si manifold is prepared using the following cleanroom process steps:

	Process Step	Tools*	Chemical Reagent	Schematic
1	Wafer clean	Wet bench	Piranha solution (H_2SO_4:H_2O_2 = 8:2)	
2	Grow thermal oxide	Thermco Tube furnace	Steam (>900 °C)	
3	CVD deposit oxide	Plasma Therm Shuttlelock PECVD system (ccp-dep)	Pressurized gases – • 5% SiH_4 in He • He • N_2O	
4	Photoresist coat	SVG Coat	Photoresists – • SPR 220–3 • SPR 220–7	
5	Expose manifold design**	MLA 150, Heidelberg Instruments	405 nm wavelength UV light	
6	Develop design	Wet bench	MF-26A (2% TMAH)	
7	Silicon oxide etch	Oxford RIE	Pressurized gases – • CHF_3 • SF_6	
8	Backside lithography + SiO_2 etch (5, 6, 7)			
8	Deep Si etch	Plasma Therm Versaline LL ICP Deep Si etcher	Pressurized gases – • CF_4 • SF_6	
9	Sputter protective Al layer	Lesker Magnetron Sputter	Al target	
10	Attach carrier wafer	Headway Spinner	Crystalbond 509 solution in acetone	

(*Continued on next page*)

Continued

	Process Step	Tools*	Chemical Reagent	Schematic
11	Backside deep Si etch	Plasma Therm Versaline LL ICP Deep Si etcher	Pressurized gases – • CF_4 • SF_6	
12	Clean wafer, separate carrier wafer	Wet bench	• Acetone • HF	 Final Manifold Structure

*Tool details can be found at: https://snfexfab.stanford.edu/guide/equipment.
**Two-dimensional exposure sketches to be used in Heidelberg MLA 150 are designed using CleWin 4.0.

Further details about the all-Si manifold process conditions and characterization data can be made available upon reasonable request to the lead contact.

Cu manifold preparation

For the hybrid μ-Cooler, the Cu manifold is prepared using layer-by-layer construction to produce the Cu mesh manifold. We apply a custom-made jig of stainless steel, for stacking, aligning, and sintering different layers of the manifold. The jig design was prepared using SolidWorks® software and fabricated by the UC Merced machine shop. The materials for components of the Cu manifold, copper mesh and copper shim stock, are sourced from McMaster-Carr and Trinity Brand Industries, respectively. We use a pulsed UV laser (Keyence) to pattern the layers of the manifold with ~20 μm lateral resolution.

After the UV-laser cutting step, we clean the patterned Cu mesh and Cu shim stock parts thoroughly, as received raw materials contain organic contaminants on the surface. To clean the surfaces, we soak them for 1 hour at 80 °C in an aqueous solution of 1M NaOH (Sigma-Aldrich). We then thoroughly rinse the pieces using DI water. After this step, we etch the pieces in 1% sulfuric acid (VWR) for 1 hour at 80 °C temperature. This etching step further cleans the surface and roughens it. Then, we apply a final rinse of the copper pieces in DI water and let them air dry.

After cleaning, we stack each Cu layer, and align them using the jig. We use a release layer (e.g., paper) between Cu parts and stainless-steel jig during sintering to ensure easy removal of the sintered parts. The sintering step is carried out at 800 °C for 30 mins in air with the manifold and jig buried in carbon powder to avoid oxidation of the sintered parts. The sintering step results in a monolithic Cu manifold. The manifold is then removed from the jig and cleaned using DI water. Finally, we etch the manifold in 1% sulfuric acid (VWR) and rinse with DI water.

QUANTIFICATION AND STATISTICAL ANALYSIS

The raw thermal model numerical data were generated by COMSOL Multiphysics® software. Thermal model settings and critical TEA assumptions are provided in the figure plus table legends and table footnotes.