Performance and Manufacturing of Silicon-Based Vapor Chambers

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This paper reviews recent progress in the development of silicon-based vapor chambers for heat spreading in electronic packages. Effective hotspot mitigation is an increasingly challenging issue in electronics thermal management, and the use of silicon vapor chambers creates opportunities for thermal-expansion matched, high performance heat spreaders that can be directly integrated with the semiconductor die. While silicon micro-heat pipes have been extensively studied as one-dimensional heat transport mechanisms for heat routing in semiconductor substrates, silicon vapor chambers require special consideration and different manufacturing approaches due to the different heat transport configurations involved. The following review therefore provides an overview on the evolution of silicon vapor chambers in terms of fabrication strategies and performance characterization. Particular focus is given to opportunities and challenges associated with using silicon as the vapor chamber envelope material rather than more traditional metal-based vapor chambers, such as the ability to optimize the wick geometry with greater fidelity and issues with manufacturing scalability. [DOI: 10.1115/1.4049801]

1 Introduction

For the past few decades, the microprocessor industry has sustained rapid performance growth by increasing chip-level transistor density without much penalty, successfully following the trajectory set forth by Moore's Law [1]. A concurrent increase in transistor density and heat generation has been mitigated in microprocessors through the end of supply voltage scaling and a shift toward multicore architecture strategies [2]. As devices continue to miniaturize and increase in complexity, however, even multicore processing strategies are limited by thermal concerns due to the formation of local, highly concentrated heat generation areas, or hotspots, in regions of the cores that experience more activity [3]. These hotspots can easily reach heat fluxes greater than 300 W/cm^2 in contemporary microprocessors [2], pushing the limits of conventional cooling approaches. Heat dissipation rates in other semiconductor devices such as power electronics are also continuously increasing, with future generations of electric vehicle power converters projected to generate heat fluxes as high as 500 W/cm^2 [4].

Further progress in semiconductor device performance improvement risks being impeded unless new thermal management strategies can be devised to address these challenges. In power electronics, more effective cooling to reduce the device junction temperature can lead to significant improvements in the module output power [5], potentially resulting in net energy savings. In addition to maintaining reasonable junction temperatures, improving overall temperature uniformity is also of particular importance, as high local temperatures can lead to drastic decreases in device reliability [6] and eventual failure from thermal runaway [7]. Effective hotspot mitigation is a challenging issue, as the cooling strategy must be able to remove sufficient heat while also ensuring chip-level temperature uniformity. Microchannel heat sinks, for instance, can help to achieve high heat transfer coefficients over an entire chip area [8–10], but require special design considerations such as through-plane microfluidic channels to provide high heat transfer rates at hotspots [11]. Other direct cooling strategies that target localized hotspot regions include microcontact thermoelectric coolers [12], micrograp coolers [13], and jet impingement [14]. These active removal strategies frequently require additional components to function such as external power supplies, liquid pumps, and heat exchangers, etc., creating significant burdens on overall system cost and complexity [15]. Chip power distributions may also be difficult to map a priori and can change dynamically based on the workload [16], making it challenging to have versatile localized cooling solutions that can work for a large range of scenarios.

A simpler approach for hotspot mitigation is to use an intermediary, high effective thermal conductivity heat spreader to transform the localized heat flux into a more uniform distribution before external heat rejection. A planar heat spreader can be integrated into a system at relatively low cost with minimal impact on overall system complexity [2]. Vapor chambers, or flat plate heat pipes, are highly effective heat spreaders that rely on nearly isothermal vapor transport in a sealed cavity to achieve thermal conductivities often much higher than that of solid materials [17]. The heat spreading mechanism is passive, and vapor chambers can operate as standalone devices without requiring any external components. Traditional vapor chambers and heat pipes are typically fabricated out of copper, aluminum, or other metals depending on the desired working fluid and temperature operation range [18]. Copper/water is a common combination in vapor chambers designed for electronics cooling, as copper has a high inherent thermal conductivity and can be easily machined and processed. The large coefficient of thermal expansion mismatch (CTE) between copper and the semiconductor die to be cooled, however, generally requires the use of compliant thermal interface materials (TIMs) with relatively poor thermal conductivities for the vapor chamber die attach [19]. This can lead to system-level thermal bottlenecks where the overall temperature drop remains limited by the TIM, regardless of how effective the heat spreader layer is. Overall, CTE mismatch between the die, spreader, and substrate can cause significant warpage and stress in the die, resulting in long-term package-level reliability challenges [20].

Recent progress in the development of silicon-based vapor chambers has created promising opportunities for CTE matched, high effective thermal conductivity spreaders that can potentially be packaged with semiconductor dies in a variety of new configurations. The use of silicon as the vapor chamber envelope material creates the possibility for metal bonding or direct integration of the vapor chamber with the semiconductor substrate, eliminating unnecessary thermal interfaces between hotspots and the

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Manuscript received October 15, 2020; final manuscript received December 14, 2020; published online February 18, 2021. Editor: Harry Dankowicz.

spreading mechanism. Using silicon as a vapor chamber envelope material presents a unique set of challenges compared to traditional metal-based vapor chambers, however, which could pose barriers to future large-scale adoption of the technology. This paper will thus provide a review and perspective on the current state of technology for silicon-based vapor chambers. As the operational theory behind silicon vapor chambers is not novel compared to the extensively studied field of metal-based vapor chambers, the primary focus will be on manufacturing challenges and opportunities that may arise with silicon as the envelope material.

This review is organized as follows. Section 2 provides a general overview of key vapor chamber operating principles. Section 3 summarizes experimental studies of silicon vapor chambers in literature, with a focus on the various existing manufacturing approaches. In Sec. 4, we examine areas where the precision of silicon microfabrication processes may give silicon-based vapor chambers a unique advantage over metal-based vapor chambers, such as the opportunity for detailed optimization of the porous wick structures that drive heat and mass transport within the device. Finally, we present new opportunities for chip-level hotspot management that could be enabled by silicon vapor chamber technology, and conclude with a discussion of future prospects and benchmarking against other competitive technologies.

2 Overview of Vapor Chamber Operating Principles

Vapor chambers are passive, two-phase devices that spread heat through vapor transport in a hermetically sealed cavity. The working fluid is driven to the heated region of the device above a hotspot through capillary action in a porous wick structure, where it evaporates, spreads throughout the cavity in vapor form, and then condenses on the opposing cold face of the device. The condensed liquid is then recirculated to the heated area, and the cycle repeats. Unlike heat pipes that are used for the one-dimensional transport of heat from one region to the other, a vapor chamber is used for two-dimensional heat spreading. The high effective thermal conductivity nature of the vapor chamber comes from the vapor transport in the core region, as the vapor can travel large distances with minimal pressure and subsequent temperature drop. The vapor thus acts as an extremely effective heat spreader in transforming the concentrated heat flux at the hotspot to a nearly uniform heat flux at the condenser region. Previously reported values for the vapor core effective thermal conductivity are in the range of 20,000 $\mathrm{Wm^{-1}K^{-1}}$ or higher [21], though this can be significantly reduced in ultrathin vapor chambers with core thicknesses less than 200 μm [22].

The porous wick on the evaporator side of the vapor chamber plays perhaps the most important role in the overall device operation, as it must supply sufficient liquid to the heated region while still maintaining a low thermal resistance pathway for heat transfer. A common maximum heat flux limitation of vapor chambers is the capillary dryout limit, where the capillary pressure supplied within the evaporator wick is no longer large enough to drive the liquid condensate back to the heated region [17]. The formation of a dry spot above the heated region can lead to a sharp rise in the wall temperature, potentially leading to device failure, though brief heat pulses above the capillary limit can be sustainable without complete dryout [23]. Other operational limits of vapor chambers include the boiling, sonic, and entrainment limits, though the capillary limit is the most frequently observed limitation for vapor chambers [24]. Much work has therefore been devoted to the study of various biporous and/or hierarchical porous structures that can simultaneously optimize the fluidic transport properties of the evaporator wick while maintaining a low thermal resistance [25–30]. In this area, silicon-based vapor chambers may benefit from the extensive array of silicon micromachining processes developed in the last two decades for MEMS and CMOS microfabrication.

The condenser side of a vapor chamber must fulfill two primary functions that have important impacts on design: First, a satisfactory mechanism must exist for returning liquid to the evaporator side wick, and second, condensation should ideally occur without the formation of a high thermal resistance, bulk liquid film. A few different approaches can be taken to achieve these goals. In a completely capillary-driven vapor chamber, the condenser side is also lined with a porous wick that delivers liquid back to the evaporator side wick and prevents bulk liquid film formation. The thermal resistance across the condenser wick is not as critical as the heat is spread over the entire wick area as opposed to the evaporator side hotspot, so the condenser wick dimensions may differ from the evaporator wick dimensions. More important in this case is for the viscous pressure drop across the condenser side wick to be minimal compared to the evaporator wick pressure drop in order to reduce the contribution to the capillary dryout limit. A wickless condenser may also be used if the vapor chamber is oriented to allow gravity driven flow back to the evaporator, though this may impact the thermal resistance due to the formation of a liquid film. An alternative method for liquid return while maintaining a low condensation resistance is to combine microstructured surfaces with chemical patterning to create superhydrophobic surfaces for jumping droplet liquid return [31–33]. The maximum heat flux in jumping droplet liquid return may be sensitive to the entrainment limit, however, as well as condensate transport distance constraints when the jumping must take place against gravity [34].

Finally, for the vapor chamber to function optimally, it must be evacuated of all noncondensable gases (NCGs) to prevent the formation of a diffusion barrier that inhibits vapor transport between the evaporator and condenser sides [35,36]. Proper evacuation and maintenance of a hermetic seal during repeated operation is therefore a primary challenge in vapor chamber manufacturing. The evacuation of the NCGs also results in a saturated, two-phase system inside the device, where the internal pressure increases accordingly with operating temperature. The maximum operating temperature of the device may therefore be constrained by mechanical burst pressure limitations, another challenge for brittle materials like silicon.

3 Experimental Studies of Silicon Vapor Chambers

Before we begin the discussion of existing silicon vapor chamber efforts in literature, a distinction must be made between silicon vapor chambers and silicon micro heat pipes. Silicon micro heat pipes were among the earliest passive, two-phase heat transport devices proposed for direct integration with semiconductor dies. The micro heat pipe concept was first presented by Cotter in 1984 as a convex, cusped groove where the mean curvature of the liquid–vapor interface is comparable to the inverse of the hydraulic radius for flow in the groove [37]. Multiple grooves may also be etched in an array to increase the heat transfer area. Since the initial conceptualization, a range of micro heat pipes have been fabricated in silicon wafers through various silicon etching techniques [38]. The key difference between silicon vapor chambers and silicon micro heat pipe arrays, however, is in the heat transport configuration. In a micro heat pipe array, evaporation takes place at one end of the grooves, and condensation takes place at the opposing end, typically with a 1:1 condenser to heater area ratio. The heat pipe primarily serves as a high thermal conductivity one-dimensional heat transport mechanism, and not a spreader. The term "micro flat heat pipe" has been used to refer to silicon-based devices with microscale features that rely on liquid–vapor phase change for heat transport purposes [39], though these devices do not necessarily contain any "micro heat pipes" as defined previously. Micro heat pipe arrays have been used as the evaporator side wick structure in devices used for heat spreading purposes, which may lead to further confusion in terms of nomenclature. For the purpose of this review, we will consider and refer henceforth to all silicon-based devices designed for the purpose of utilizing liquid–vapor phase change for heat spreading purposes, with a condenser to heater area ratio > 1, as silicon vapor

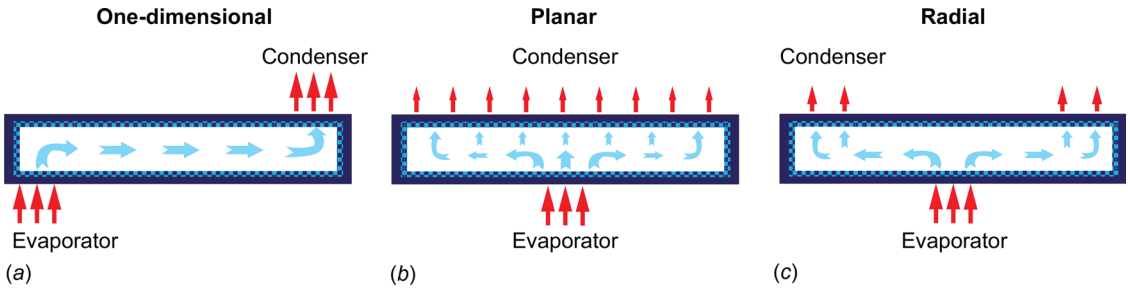


Fig. 1 (*a*) Heat pipe operation with one-dimensional heat transport. (*b*) A two-dimensional heat planar spreading configuration with a vapor chamber, where heat rejection occurs over the entire face opposite of the evaporator. (*c*) A two-dimensional radial heat spreading configuration with a vapor chamber.

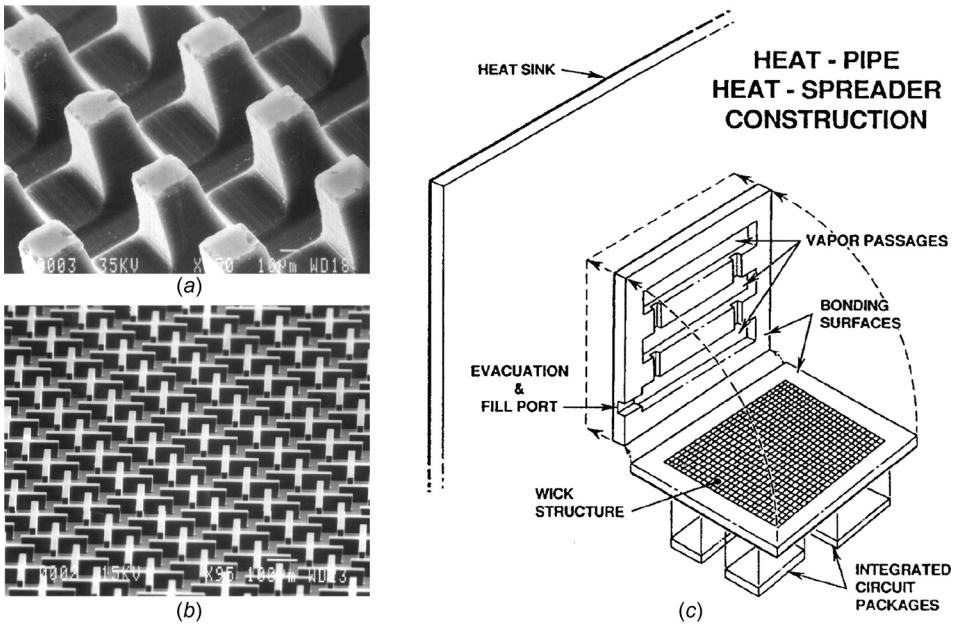


Fig. 2 (*a*) Micropillar wick structure formed in silicon using bidirectional cuts with a wafer saw. (*b*) Patterned crosses etched into silicon using deep plasma etching with a photomask. (*c*) An overall schematic of a final vapor chamber design with a wickless vapor cap wafer designed and fabricated for multichip heat spreading. (Reproduced from Benson et al. [41], © 1998, Taylor & Francis Ltd. (www.tandfonline.com). Reprinted with permission from Microscale Thermophysical Engineering.)

chambers. Figure 1(*a*) shows an example of a heat pipe used for one-dimensional heat transport for comparison with vapor chambers as defined in this review used in various planar (Fig. 1(*b*)) and radial (Fig. 1(*c*)) spreading configurations. Silicon vapor chambers can still leverage much of the manufacturing progress demonstrated from silicon micro heat pipe literature, but present a unique set of considerations due to the different heat transport geometry.

3.1 Silicon Vapor Chamber Manufacturing Approaches. In the simplest possible manifestation of a silicon vapor chamber, the vapor chamber can be fabricated from a minimum of two silicon wafers, with the evaporator side and corresponding wick structure formed on one wafer, and the condenser side located on the other. The evaporator wick can be created by either etching a pattern directly into the silicon to form a monolithic wick, or by depositing another material on top of the silicon. As mentioned in Sec. 2, a wick is not necessarily required on the condenser side, though the absence of one does render the device operation orientation-dependent. In low-gravity or antigravity orientations, liquid pooled on the condenser surface will not effectively drip back to the evaporator side without a wick structure. For applications where antigravity orientations are not required, a wickless condenser configuration may be preferred as the vapor cavity etch can be confined entirely to the condenser wafer.

Benson et al. performed some of the earliest investigations of silicon vapor chambers as heat spreading substrates for multichip modules at Sandia National Laboratories [40,41]. Before these works, the fabrication of liquid wicking structures in silicon was primarily devoted to creating rectangular or triangular grooves that could be utilized for one-dimensional transport in micro heat pipe arrays [42]. Benson et al. determined based on modeling that the ideal wick structure dimension for a vapor chamber application with alcohol as the working fluid would range from 50 to 75 μm [40], and used a variety of different approaches to explore silicon wicks that could be used for two-dimensional liquid transport. As seen in Fig. 2, Benson et al. fabricated different two-dimensional wick patterns such as pillar arrays using bidirectional cuts with a wafer saw (Fig. 2(*a*)), and patterned crosses through deep plasma etching with a photomask (Fig. 2(*b*)). A 250 μm deep well was etched into a second wafer with potassium hydroxide (KOH) to form the vapor cavity. The wickless vapor cap wafer was then joined to the evaporator side wick structures with a silica

glass bond to serve as the condenser. A schematic of the final device is shown in Fig. 2(*c*), as well as the multichip heat spreading concept that motivated the development of the silicon vapor chamber. The active area of the final vapor chamber was 3.8 × 3.8 cm^2.

Gillot et al. utilized rectangular grooves and a triple stack process to create a silicon vapor chamber capable of operating in antigravity orientations [43]. A schematic of the vapor chamber design is shown in Fig. 3(*a*). Arrays of rectangular grooves (SEM shown in Fig. 3(*b*)) were etched into the top and bottom wafers with deep plasma etching to form the condenser and evaporator wick structures. The two wafers were then bonded to an intermediary etched-through wafer with a silicon direct bonding process to form the vapor cavity. Vertical grooves visible around the periphery of the vapor cavity acted as liquid condensate return structures between the condenser and evaporator. The use of three separate wafers allowed for the wick and vapor cavity etches to be confined to separate wafers, eliminating the need for more complicated multiheight etching processes in a single substrate. Other studies have taken similar triple stack approaches to accommodate monolithic wick structures on both the condenser and evaporator sides of the device [44,45].

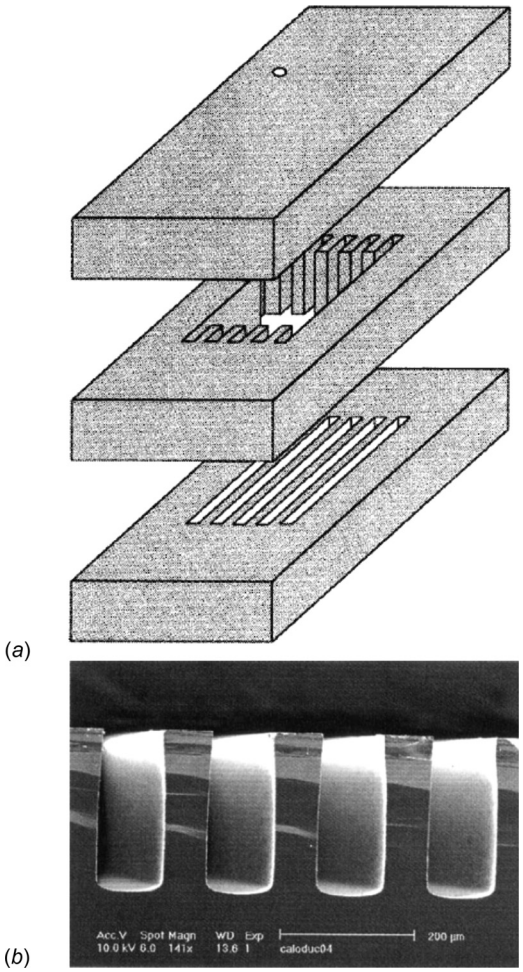


Fig. 3 (*a*) A triple stack silicon vapor chamber configuration with grooves etched into the condenser and evaporator sides to enable operation in antigravity orientations. The vapor cavity is contained within the intermediary insert wafer. (*b*) A scanning electron microscope (SEM) image of the rectangular grooves used for liquid transport within the vapor chamber. (Reproduced from Gillot et al. [43], © 2003, IEEE. Reprinted with permission from IEEE Transactions on Components and Packaging Technologies.)

Cai et al. fabricated a "hexcell" silicon vapor chamber with condenser and evaporator wick structures using just two silicon wafers that were 1 mm thick each [46]. The hexcell was named as such due to the hexagonal shape of the final device, which was meant for use as a scalable unit cell that could be bonded to other hexcells to create a larger array of silicon vapor chambers. A cross-sectional image of the final bonded device is shown in Fig. 4(*a*). The authors reported using a multiple mask exposure lithography process with various resist mask thicknesses to create the wick structures and sidewall condensate return structures in a single etching process. Further details of the wick and cavity formation process were not given, though the authors list dry etching as a primary fabrication step for the device. The etched wafers were bonded together with an Au/Si eutectic bond and then diced to release individual hexcells. The sidewalls of the individual hexcells were metalized with a titanium adhesion layer and 2-μm-thick platinum layer, then soldered together to form larger hexcell arrays. An image of a sidewall-bonded hexcell array is shown in Fig. 4(*b*), where the individual hexcells have edge lengths of 1 cm and total area of 2.6 cm^2.

Other approaches that have demonstrated the ability to create monolithic condenser and evaporator wick structures without the need for a separate vapor cavity wafer include ultraviolet (UV) laser ablation. Liu et al. used a 500-μm-thick wafer as the condenser substrate and a 1 mm thick evaporator wafer to contain both the vapor cavity and evaporator micropillar structures [47]. The UV laser ablation was able to etch the vapor cavity and micropillar structures into the 1 mm thick wafer with a single, lithography-free process. After laser ablation to form the vapor cavity and corresponding wicks, the two substrates were bonded together using a glass frit. The laser ablation process also generated a conformal microscale roughness over the wick structure that was reported to increase the area for thin-film evaporation from the evaporator wick, potentially by up to a factor of 3. A top view of the microscale roughness generated over the micropillar

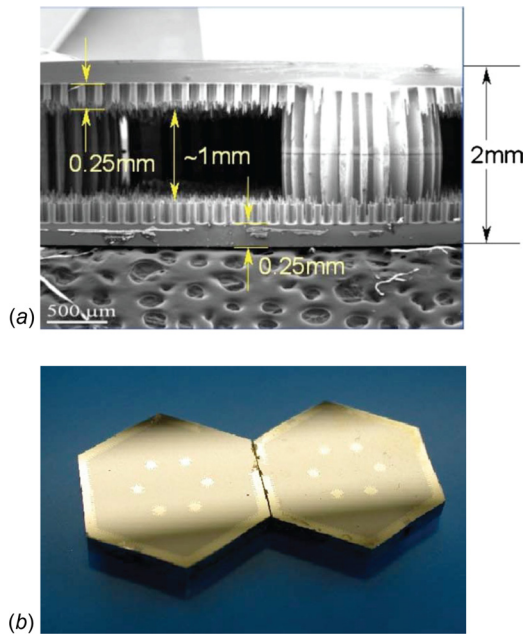
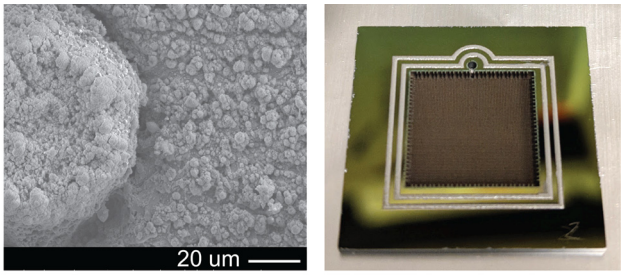


Fig. 4 (*a*) Cross sectional image of a silicon vapor chamber with micropillar wicks on the condenser and evaporator surfaces fabricated with a two-substrate approach. A multiple mask exposure lithography process with various resist mask thicknesses was used to create the wick structures and sidewall condensate return structures in a single etching process. (*b*) An image of two "hexcell" vapor chambers soldered together after metallizing the sidewalls with a 2-μm-thick platinum layer. (Reproduced from Cai et al. [46].)



(*a*) (*b*)

Fig. 5 (*a*) A top view of an SEM image showing the conformal microscale roughness generated over micropillar structures fabricated with UV laser ablation. (*b*) The vapor cavity and micropillar wick etched into a single substrate with a lithography-free process using laser ablation. Glass frit bond lines are printed around the edge for joining to a condenser substrate. (Reproduced from Liu et al. [47].)

structures with laser ablation is shown in Fig. 5(*a*), and the etched cavity and pillars with printed glass frit bonding lines is shown in Fig. 5(*b*). One downside of fabrication with laser ablation, however, is that the ablation process can lead to the formation of silicon debris at the edges of etched cavities. Glass frit bonding was therefore used in this study as opposed to other silicon bonding methods such as Au/Si eutectic that have relatively stricter requirements for the smoothness of bonding surfaces. Masking the silicon with polydimethylsiloxane (PDMS) has been suggested as a strategy to prevent this issue of debris formation in future silicon devices processed with laser ablation [48].

Nonmonolithic wick structures have also been integrated with silicon substrates to reduce the silicon etching process requirements to just a single step to form the vapor cavity. Liang et al. followed this approach by etching the silicon vapor cavity first, then depositing copper powder on top of adhesive dot arrays patterned with inkjet printing to form the evaporator wick [49]. Images of the adhesive dot arrays patterned on top of the silicon substrate with various porosities are shown in Figs. 6-(1-3)(*a*), and the corresponding wick structures after copper powder deposition are shown in Figs. 6-(1-3)(*b*). Close up SEM images of the copper powder structures are shown in Figs. 6-4 and 6-5. While this approach simplified the required etching processes, it also introduced the possibility of poor thermal interfaces and/or CTE mismatch between the wick and the substrate. Long term reliability of the various bonding interfaces must therefore be taken into account when using nonmonolithic wick structures.

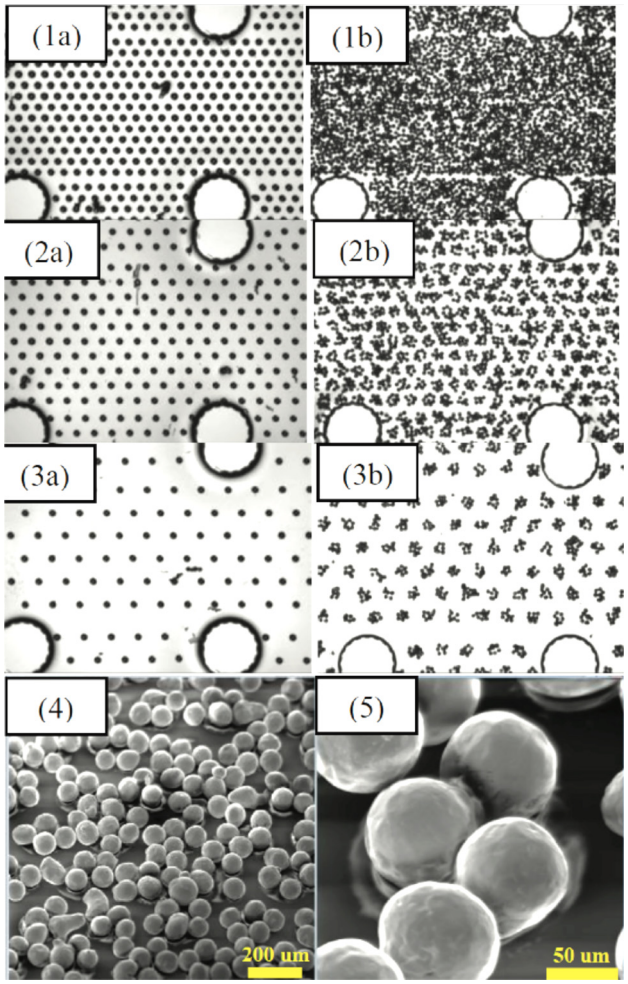


Fig. 6 (1-3)(*a*) Adhesive dot arrays of varying porosity printed into a silicon cavity with inkjet print. (1-3)(*b*) Copper particle wick formed on top of adhesive dot arrays with varying porosity after depositing copper powder into the cavity. (4) SEM image of copper wick with porosity of 0.66. (5) Close up view of copper particles for wick with porosity of 0.66. (Reproduced from Liang et al. [49], © 2017, IEEE. Reprinted with permission from IEEE Proceedings.)

3.2 Liquid Charging and Evacuation Strategies. The following two goals act as primary design guidelines to determine appropriate charging and evacuation strategies for producing silicon vapor chambers. One, the vapor chamber must be evacuated of all noncondensable gases and remain hermetically sealed for the duration of the vapor chamber lifetime. The components comprising the vapor chamber must not react to form additional noncondensable gases with time. Second, vapor chamber and heat pipe operation is highly dependent on the volume of charged working fluid [50–53]. The manufacturing process must therefore be able to consistently deliver the same amount of working fluid to each device, within an appropriate precision level dependent on the overall volume of the vapor chamber.

The entirety of the silicon vapor chambers studied in literature thus far have followed the same general liquid charging and evacuation approaches, where the substrates are bonded together under dry conditions, and one or more through-holes are left open for subsequent evacuation and charging procedures. After bonding, external charging tubes are attached to the through-holes by either soldering to a metalized area around the port surface [43,46,54,55], or joining with epoxy [47,49]. The vapor chamber is then evacuated of noncondensable gases and charged with working fluid that has typically also been degassed prior to charging. Liu et al. used a slightly different approach in order to more accurately measure the amount of liquid charge volume for their miniature $1 \times 1\,\text{cm}^2$ silicon vapor chamber, which required a charging precision of the order of microliters [47]. For that purpose, they charged the device with liquid first, measured the mass differential before and after charging to obtain the precise level of liquid charge volume, then evacuated the chamber and degassed the liquid with a two-step vacuum procedure.

A range of dry silicon wafer bonding methods have been demonstrated for vapor chamber fabrication, including glass frit [45,47], Au/Si eutectic [50,56], direct silicon fusion bonding [43], anodic bonding [57], and spin-coated epoxy [49]. The choices of bonding and charging tube attachment methods can have important implications for various other components of the fabrication process. As an example, direct silicon fusion bonding requires no intermediary bonding material, but may need temperatures as high as 1100 °C to form a solid bond [58]. This could potentially preclude the use of any nonsilicon materials in the vapor chamber fabrication process that would be damaged at such high temperatures. Metallization for solder port surfaces, for example, would possibly need to be performed after the bonding step.

Additionally, any bonding layers or charging port materials must be chemically compatible with the vapor chamber working fluid and have minimal outgassing. For this reason, wafer bonding or charging tube attachment with epoxies may be less likely to be viable long-term solutions outside of laboratory-level experiments. Finally, another important item to consider for future processes is the CTE compatibility of any nonsilicon materials used during vapor chamber fabrication. A soldered charging tube attachment, for example, could potentially lead to reliability issues if subjected to significant cycles of thermal expansion. Selective placement of the charging port to minimize temperature rise during thermal cycling may therefore be a relevant future design consideration.

Overall, the silicon vapor chambers considered thus far have all been degassed and charged with liquid at the individual device level. This is beneficial for laboratory characterization purposes, as it allows for experimental iteration to find the optimal liquid charge volume. Using external charging tubes also allows the vapor chambers to be easily connected to equipment such as syringe pumps for liquid charging and vacuum pumps for NCG evacuation. For silicon vapor chamber technology to be readily scalable, however, it may be beneficial to develop liquid charging and evacuation procedures that could be performed on a wafer-scale as opposed to individual device level. A discussion of some possible wafer-level charging, evacuation, and bonding procedures will be discussed Sec. 6.

3.3 Performance Characterization of Silicon Vapor Chambers. Unlike heat pipes with one-dimensional heat flow, an effective thermal conductivity cannot be readily defined for vapor chambers without comparative numerical simulations due to the two-dimensional nature of the heat spreading. Cai et al. fabricated a silicon device meant for use as a vapor chamber, but experimentally characterized it as a one-dimensional heat pipe to more easily obtain an effective thermal conductivity value [45]. It is important to note that the effective thermal conductivity value calculated in this scenario (2500 $Wm^{-1}K^{-1}$) [45], however, cannot be directly applied to the device performance if used as a vapor chamber due to the different heat flow configurations involved. A direct comparison of the relative performance of various silicon vapor chambers is also difficult as the different form factors and hotspot to condenser area ratios lead to different innate spreading resistances. Results have sometimes been reported in terms of performance improvement of the vapor chamber with and without working fluid [43,56], but this metric only provides confirmation that the vapor chamber is functioning, with minimal information on the degree of functionality. Another method reported in literature has been to compare the vapor chamber performance relative to a benchmark solid spreader, frequently that of silicon. This metric can provide perhaps the most consistent characterization approach, especially if the solid benchmark spreader is chosen to have dimensions equal to the vapor chamber.

Benson et al. investigated the thermal performance of their vapor chamber using an infrared (IR) measurement technique [41]. A 0.57 cm^2 test die was utilized as the heat source and attached to the center of the evaporator side of the vapor chamber. The authors estimated the effective thermal conductivity of the vapor chamber with methanol as the working fluid to be approximately 800 $Wm^{-1}K^{-1}$ based on the ratio of the temperature gradient at the heater location compared to a vapor chamber with no working fluid. More extensive data was not provided to confirm this effective thermal conductivity estimate, though it was promising as an initial result that silicon vapor chambers could be utilized as high performance heat spreaders. The authors also hypothesized that partial dryout may have occurred for power inputs above 5 W (corresponding to a heat flux of 15 W/cm^2).

Ivanova et al. designed a vapor chamber meant for spreading heat from discrete components to a surrounding metal chassis (Fig. 7(*a*)) in a radial as opposed to planar configuration [44]. The

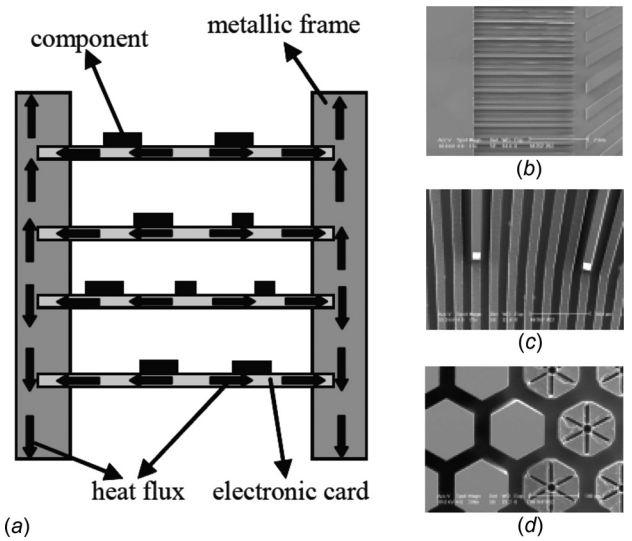


Fig. 7 (*a*) Concept drawing of a silicon vapor chamber used to spread heat from multiple electronic components to a peripheral metallic frame. (*b*) Rectangular grooves lining the edges of a silicon vapor chamber to act as the condenser zone in a radial heat spreading configuration. (*c*) Radial grooves used to provide the liquid return pathway from the condenser zone to (*d*) hexagonal pillars in the heated region. (Reproduced from Ivanova et al. [44], © 2006, IEEE. Reprinted with permission from IEEE Proceedings.)

wick design included specific features to account for a peripheral condenser region and was separated into three distinct zones. A fine-featured array of rectangular grooves lining the edges of the vapor chamber served as the condenser zone (Fig. 7(*b*)), and a radial groove array (Fig. 7(*c*)) provided the liquid return pathway from the condenser zone to the heated region, which was covered with an array of hexagonal pins (Fig. 7(*d*)). The wick was separated into these distinct zones to provide a low flow resistance pathway through the radial grooves to supply the low thermal resistance hexagonal pin region in the heated area. During experiments, a 1 × 1 cm^2 thin-film copper resistor deposited onto a silicon substrate was glued to the center of the evaporator to serve as the heat source. A copper cold plate was mounted to a 5 mm wide area around the periphery of the vapor chamber to create the condenser zone. The silicon vapor chamber showed a more than 60% improvement in thermal resistance and 40% reduction in maximum temperature compared to a solid silicon plate of comparable dimensions for a heat input of approximately 10 W. The authors supplied up to 75 W of input power without observing any noticeable change in the device thermal resistance, leading to the conclusion that no dryout limit had yet been reached. Due to maximum temperature limitations on the resistor used as the heat source, higher powers were not explored. A numerical model of the pressure drop in the radial grooves concluded that at least 120 W could be dissipated with this kind of structure before reaching the capillary dryout limit.

Kang et al. fabricated a 5x5 cm^2 vapor chamber with a triple stack process and used a radial array of trapezoidal grooves as the evaporator wick. A total of 70 grooves were patterned on the condenser and evaporator surfaces, with etched depths of approximately 160 μm each. The thermal performance was characterized by using a 1.1 cm^2 silicone heater glued to the evaporator center as the heat source, and measuring the temperature distribution along the condenser and evaporator surfaces as a function of heat input with various thermocouples. The device was tested in a planar heat spreading configuration, where the heat from the source was spread over the entire opposing condenser area and rejected to a copper cold plate. The thermal performance of the device was found to vary strongly as a function of the liquid charge volume.

Overall, the vapor chamber was able to reduce the evaporator side temperature by approximately 8-27% depending on the liquid charge amount for a maximum power input of 27 W. A 70% liquid fill ratio with water as the working fluid was found to have the best thermal performance. The maximum heat transfer limitation of the device was not explored.

A number of other studies also reported a strong dependence of the vapor chamber thermal performance on liquid charge volume [47,49], which is in agreement with observations from general heat pipe literature [17]. A key takeaway from these studies is that vapor chambers of different internal volumes will require different levels of charging precision. For the previously discussed vapor chamber tested by Kang et al., the optimal fill ratio of 70% corresponded to a liquid charge volume in the range of hundreds of microliters, assuming the fill ratio was defined based on the total internal volume of the vapor chamber [50]. Based on their results, a difference in fill ratio of 17% led to an approximately 6% change in maximum temperature, resulting in an overall sensitivity of roughly 3% change in fill ratio for every 1% increase in temperature. For an absolute liquid charge volume of approximately 500 μL, this would result in an absolute charge volume sensitivity of 15 μL per 1% increase in temperature. The results of Liu et al. for the miniature $1 \times 1\,\text{cm}^2$ vapor chamber showed a more than 200% increase in thermal resistance when the total liquid charge volume was increased from 11.9 to 20.3 μL [47]. The recommended liquid charging precision in this case was of the order of $\pm 2\,\mu$L. Overall, these results indicate that a charging precision of the order of at minimum 10-15% of the total charge volume may be desirable in order to observe the impact of liquid charge on overall thermal performance. These guidelines should therefore be taken into consideration when considering future manufacturing approaches for silicon vapor chambers, as different form factors may require different charging processes with varying levels of control.

Table 1 presents a summary of experimental characterizations of silicon vapor chambers in literature in terms of their form factors, hotspot to condenser area ratios, wick structures, reported performance metric, and range of power inputs. A few general trends emerge when considering the summary in Table 1. First, the vapor chambers are typically much larger than a standard die size, with total areas ranging from 5 - 25 cm^2. From a heat spreading perspective, it is beneficial to reduce the heat flux as much as possible by spreading to a much larger area. From a cost perspective, however, this could potentially result in silicon vapor chambers that cost significantly more than a typical semiconductor die, primarily due to the substantially larger silicon substrate area required as well as cost of additional processing steps. Larger silicon vapor chambers may therefore be better suited for multichip spreading applications, and smaller area vapor chambers could be more appropriate for die-matched heat redistribution. Overall package cost and performance tradeoffs will have a significant impact on whether or not a silicon vapor chamber is suitable for a particular application, and a more detailed discussion of this will be presented in Sec. 6.

From Table 1, water also emerges as the predominant working fluid of choice. Water is easy to work with in a laboratory setting and has a relatively high capillary merit number [22], where

$$M_l = \frac{\sigma \rho_l h_{fg}}{\mu_l} \tag{1}$$

The merit number represents the potential of the working fluid to maximize the capillary dryout limit in the vapor chamber. A higher surface tension, σ creates a higher capillary pressure in the wick, while a higher density ρ_l and latent heat h_{fg} result in a lower evaporative mass flux for the same heat input. A lower liquid viscosity, μ_l leads to a lower viscous pressure drop. Overall, water tends to have a merit number approximately 10 times higher than other working fluids in the 0 °C–200 °C operating range [17].

Table 1 Summary of experimental characterizations of silicon vapor chambers in literature

Authors	Vapor chamber area	Hotspot to condenser area ratio	Tested heating configuration	Wick structure	Performance metric	Max input power	Initiation of dryout	Working fluid
Benson et al. [40,41]	$3.8 \times 3.8\,\text{cm}^2$	1:25	Planar	Crosses	Estimated effective thermal conductivity ~ $800\,\text{Wm}^{-1}\text{K}^{-1}$	15 W	5 W	Methanol
Liang et al. [49]	$2 \times 2\,\text{cm}^2$	1:36	Radial	Biporous monolayer copper powder	Thermal resistance ~18% improvement over solid Si	1.6 W	0.9 W	Water
He et al. [56]	$3 \times 3\,\text{cm}^2$	1:9	Planar	Micropillars	Thermal resistance ~50% improvement over empty chamber	37 W	13 W	Water
Wei et al. [61]	$3 \times 3\,\text{cm}^2$	1:9	Planar	Micropillars	Maximum dryout power of 98 W	98	98	Water
Kang et al. [50]	$5 \times 5\,\text{cm}^2$	1:25	Radial	Microgrooves	Evaporator temperature ~27% improvement over solid Si	27 W	N/A	Water
Gillot et al. [43]	$0.9 \times 5\,\text{cm}^2$	1:5	Planar	Microgrooves	Thermal resistance ~45% improvement over empty chamber	30 W	N/A	Water
Ivanova et al. [55]	$1 \times 5\,\text{cm}^2$	1:5	Planar	Microgrooves	Thermal resistance ~65% improvement over empty chamber	60 W	20–30 W	Water
Ivanova et al. [44]	$5 \times 5\,\text{cm}^2$	1:9	Radial	Microgrooves	Thermal resistance ~66% improvement over solid Si	75 W	N/A	Water
Cai et al. [45]	$4 \times 4\,\text{cm}^2$	1:1.25	One-dimensional	Micropillars	Effective thermal conductivity in 1D mode ~ $2500\,\text{Wm}^{-1}\text{K}^{-1}$	10 W	10 W	Ethanol
Liu et al. [47]	$1 \times 1\,\text{cm}^2$	1:10	Planar	Micropillars	Hotspot temperature uniformity ~45% improvement over solid Si	10 W	N/A	Water

The chemical compatibility of water with silicon vapor chamber components is therefore an important consideration in the overall vapor chamber design. Of primary concern is whether or not water will react with the various vapor chamber materials to form noncondensable gases. Potential sources include the corrosion of solders used for external tube attachment and/or oxidation of pure silicon by water to form hydrogen gas. Cai et al. performed a detailed investigation of the chemical compatibility of various solders and recommended predominantly lead-based solders for better corrosion resistance [59]. Artificially thickening the native SiO_2 layer on a freshly fabricated silicon vapor chamber sample was also described as a potential method to prevent further oxidation of the silicon from water during operation [59].

Note that besides the capillary merit number, another figure of merit that can contribute to vapor chamber working fluid selection is the vapor merit number, M_v [60]. M_v depends on the thermophysical properties of the working fluid in vapor form and prioritizes the effective thermal resistance of the vapor core, as opposed to the dryout limit considered in M_l. Working fluid choice based on this vapor figure of merit can become more critical when the vapor core thickness approaches the ultrathin regime, and the vapor core resistance begins to dominate the total stack resistance [22]. Future silicon vapor chambers limited by the vapor core resistance may therefore have requirements for chemical compatibility with working fluids other than water.

In general, when the comparison was provided, the studied silicon vapor chambers showed significant improvement in heat spreading performance over solid silicon benchmarks. The maximum input power limitation was not extensively studied, however, and the summary in Table 1 shows a large variation in reported input powers ranging from as low as 1.6 W to 70 W. Taking into account the different heater sizes used in the studies, the different input powers can be translated to a heat flux range of approximately 13–100 W/cm^2. Some studies identified a maximum capillary-limited dryout power, though this was not listed for all cases, and a number of studies reported that exploring higher heat fluxes was not possible due to maximum temperature limitations of various experimental components [44,47]. Overall, quantification of the maximum input power/heat flux for a vapor chamber is a critical parameter to determine what kind of heat spreading applications the device can be utilized for. The capillary-limited dryout power in vapor chambers is a strong function of the overall vapor chamber dimensions, and in particular depends on the design of the evaporator wick. To gain more perspective on this topic, the following section will provide a more in-depth look at fundamental studies on the capillary-fed evaporation and boiling performance of various porous materials that can potentially be used as evaporator wicks in silicon vapor chambers.

4 Porous Wick Fabrication and Optimization Strategies

As mentioned previously, the evaporator wick provides perhaps the most important function in a vapor chamber. To prevent capillary dryout, the wick must be able to supply enough capillary pressure to drive fluid to the heated region while maintaining a low viscous pressure drop. The latter requirement is satisfied by the structure having a high fluid permeability. The permeability of a porous material is roughly proportional to the square of the medium's characteristic length scale [62], or

$$K \propto \delta^2 \tag{2}$$

Depending on the composition of the porous material, the definition of the characteristic length scale varies. The permeability of sintered copper wicks comprised of packed particles, for example, depends primarily on the particle size [63] while inverse porous materials are more commonly defined by a characteristic pore size [64].

The capillary pressure of the wick is typically proportional to the inverse of the characteristic length scale, or

$$P_c \propto \frac{1}{\delta} \tag{3}$$

This conflicts with the desired scaling trend for enhancing permeability. Additionally, the wick should have a low thermal resistance to minimize the temperature drop between the vapor chamber wall and vapor region. A majority of the evaporation in porous microstructures has been demonstrated to occur from a thin liquid film region of the three-phase contact line of the order of 1–10 μm thick [65–67]. Increasing the surface area to volume ratio is therefore an important consideration in wick design to maximize the area available for evaporation from the thin liquid film region [68]. The initiation of boiling within the wick can also reduce the wick resistance due to the intensive phase-change processes accompanying bubble nucleation and departure [69]. In groove-based wicks, however, the formation of vapor bubbles leads to an almost immediate blockage of available liquid flow channels and rapid dryout, marking the initiation of boiling as a maximum operational heat flux [70]. With other types of wick structures, boiling can be sustained for a larger range of heat input, though the formation of vapor within the wick can still inhibit the liquid flow and reduce the effective permeability of the wick below the single-phase value [71]. The maximum heat flux limitation of the evaporator wick structure therefore depends on multiple factors such as the wick thickness, pore network structure, wick area, and absence or presence of boiling [71–73]. These various considerations lead to a multi-objective design problem for the evaporator wick, where combinations of structures with varying characteristic dimensions may be desirable for the best overall performance. In this realm, silicon vapor chambers may stand to benefit from the various MEMS processes available for silicon micromachining, enabling greater flexibility in the thermofluidic design and optimization of the evaporator wick structure.

4.1 Monolithic Silicon Wicks. Standard photolithography combined with anisotropic etch processes such as deep-reactive-ion-etching can produce a wide range of structures in silicon. The advantages of such an approach include monolithic integration of the wick with the substrate, removing any potential issues of thermal boundary resistance, and almost infinite possibilities for different combinations of geometric shapes due to the ease of patterning with photolithography. Previously mentioned examples of such monolithic wick structures implemented in silicon vapor chambers include crosses [40] as well as rectangular and radially patterned groove arrays [43,50].

Perhaps the most extensively studied monolithic silicon wick structure for vapor chamber applications, however, has been silicon micropillar arrays [45,74–78]. The regular geometry of micropillar arrays makes them conducive to unit-cell modeling approaches for both the fluid flow and heat transfer, enabling relatively accurate model-based prediction of key parameters such as wick permeability and dryout heat flux [74,79–82]. A schematic of the typical meniscus distribution in a heated micropillar array with diameter d, pitch p, and height h is shown in Fig. 8. As liquid flows from the outer edge of the wick toward the center, the meniscus shape becomes increasingly concave due to evaporation from the vapor–liquid interface. The variation in capillary pressure along the wick thus drives the liquid flow from the edge to the heated region. The minimum sustainable contact angle between the liquid and the micropillar surface corresponds to the receding contact angle for the liquid/solid combination; for heat fluxes above this, the meniscus is no longer stable and dryout occurs [27,80].

Biporous structures with nonhomogeneous patterns of silicon micropillars can increase the dryout heat flux and reduce the wick thermal resistance. As shown in Fig. 9(*a*), Coso et al. combined square-packed micropillars with microchannels (30–60 μm in width) to reduce the viscous pressure loss across the wick while maintaining high capillary suction within denser micropillar

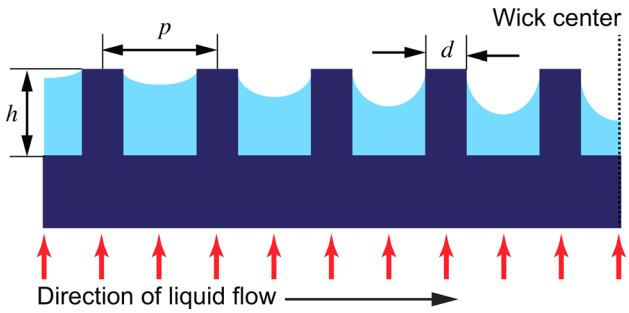


Fig. 8 Liquid distribution in a heated micropillar wick. The liquid meniscus becomes increasingly concave near the center of the wick due to evaporation from the vapor–liquid interface. Dryout occurs when the minimum sustainable contact angle between the liquid and the micropillar surface corresponds to the receding contact angle for the liquid/solid combination.

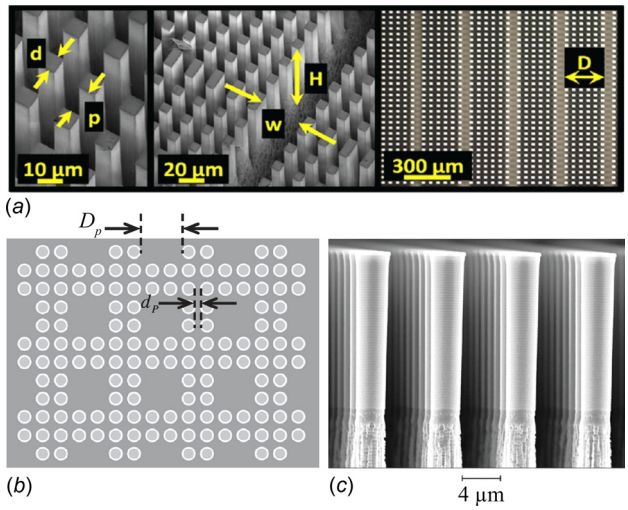


Fig. 9 Examples of biporous/hierarchical silicon wick structures. (*a*) Biporous micropillar array with 30-μm-wide microchannels interspersed between denser micropillar arrays for liquid feeding (Reproduced from Coso et al. [27]). (*b*) Micropillar arrays interspersed with square cavities that demonstrated a 31% increase in capillary performance over a homogeneous array. (Reproduced with permission from Byon et al. [83], © 2014, Elsevier). (*c*) Bi-roughness micropillars fabricated with a two-step DRIE process (Reproduced with permission from Azarkish et al. [85], © 2014, IOP Publishing).

arrays ($d = 3$–$29\,\mu$m, $p = 5$–$28\,\mu$m, $h = 56$–$243\,\mu$m) [27]. The thickest wick with a micropillar height of 243 μm was able to sustain a maximum heat flux of up to 277 W/cm^2 for a heated area of 1 cm^2, with a stable nucleate boiling regime of 185 W/cm^2 beyond the boiling incipience heat flux [27]. Similarly, as shown in Fig. 9(*b*), another approach by Byon et al. involved interspersing larger square openings into a denser micropillar array to increase the porosity of the wick [83]. The capillary performance was found to improve over a homogeneous array by more than 30%.

Other micropillar optimization strategies have included texturing the surface of the pillar to enhance the area for thin-film evaporation. As mentioned in Sec. 3.1, Liu et al. were able to generate a conformal microscale roughness over silicon micropillars fabricated through UV laser ablation [47]. In addition to increasing the area for thin-film evaporation, Hazra et al. also found in another study that the conformal surface roughness could enhance the capillary performance of laser ablated micropillars by more than 100% over smooth pillars [84]. A downside of the laser ablation process, however, was that the minimum feature size was limited to approximately 70 μm. Azarkish et al. utilized two different DRIE recipes to create a bi-roughness micropillar array as shown in Fig. 9(*c*) [85]. The bi-roughness micropillar configuration was designed for use as a micro-evaporator in chip scale Rankine cycle applications and demonstrated a 52-122% improvement in evaporation rate over smooth silicon micropillars.

4.2 Wicking Structures Made From Materials Other Than Silicon. In addition to monolithically fabricated wicks in silicon, porous structures composed of other materials grown on top of or bonded to silicon substrates may also be promising wick configurations. Some advantages to using other materials such as metals include the possibility of a higher thermal conductivity contribution to the solid wick fraction, potentially reducing the overall wick resistance, and further possibilities for multilayered, three-dimensional porous structures. Disadvantages include additional fabrication steps needed to bond/grow additional material onto the silicon substrate, and any associated reliability issues with a poor bonding interface or thermal expansion mismatch. Here, we provide a brief overview of some porous structures comprised of materials other than silicon that could be integrated into future silicon vapor chambers.

Copper is an appealing wick material choice due to its high inherent thermal conductivity, and sintered copper in particular has been extensively studied as a wick structure for traditional copper-based heat pipes and vapor chambers [25,30,63]. The sintering process to form a connected wick from discrete copper powder, however, requires very high temperature processing ($>$ 800 °C) [86] and can result in a wide range of effective wick thermal conductivities depending on the sintering conditions [87]. Such high temperatures are incompatible with many semiconductor applications and would limit potential packaging integration scenarios for silicon vapor chambers. Additionally, the relatively large powder particle size ($>$ 50 μm) used in previous studies results in large wick thicknesses ($>$ 500 μm) [70] that fall beyond the ideal range of length scales associated with silicon wafer processing.

A potentially more compatible method to form copper/other metal based wicks on silicon substrates is through electrochemical processes, which have a long history of widespread use in MEMS devices for low-cost, low-temperature, and scalable growth of metal layers of varying compositions [88,89]. To create a porous metal structure with electrodeposition, the substrate of interest must have an electrically conductive surface. This can be achieved on silicon by using highly doped wafers [90] or evaporating/sputtering a thin metallic layer on the surface of interest to act as a conductive seed layer. The use of a template or pattern over the seed layer or conductive area then defines the shape of the resulting porous metal film after electroplating. Copper inverse opals are one example of porous metal films fabricated through a templated electrodeposition process that have demonstrated great promise for use as evaporative wicks [71,91,92]. The highly ordered, three dimensional porous network is fabricated by using self-assembled polystyrene spheres to form a template, electroplating through the template, then dissolving the polystyrene with an organic solvent to create the resulting inverse opal structure [93]. Extremely high critical heat flux values ($>$ 1 kW/cm$^{2)}$ have been reported for such structures with very low superheat ($<$ 15 °C), albeit for small wicking lengths ($<$ 200 μm) [71]. Additional high permeability fluidic structures integrated with the inverse opals could be a promising route to scale up the inverse opal thermal performance to the millimeter length scales required for use in a vapor chamber wick, similar to the approaches used in biporous silicon micropillar wicks [83]. Hierarchically structured copper micropillars electroplated on silicon substrates have also been studied as potential high performance wicking materials [94,95]. To increase the wettability of water on copper, Nam et al. used a chemical oxidation scheme to form a conformal superhydrophilic nanostructure on top of the copper micropillar [95]. The nanostructuring was found to improve the dryout heat flux by over

70% compared to bare micropillars, reaching a maximum heat flux of approximately 200 W/cm^2 over a 5 × 5 mm^2 heated area. Other intricate structures that have been fabricated through electroplating on various substrates include Cu meso-lattices formed by direct laser writing of 3D patterns into photoresist [96], though the efficacy of such structures in capillary fed evaporation/boiling has not been thoroughly studied.

Additional potential wick structures that can be fabricated on silicon substrates include various nanowire/nanotube arrays. Carbon nanotubes (CNTs) are particularly of interest, as vertically aligned films of varying heights can be directly grown on silicon substrates with relative ease [97]. Some additional attractive attributes of CNTs include the possibility of functionalization to create hydrophilic surfaces [98] and high axial single tube thermal conductivities of approximately ~2000 Wm^{-1}K^{-1} [99] (though this has been shown to be highly dependent on the CNT growth quality [100]). The nanoscale pores of the nanotube arrays can generate very high capillary pressures within the wick, but can also lead to large viscous flow resistances that prevent uniform CNT arrays from being used as the sole wicking material. Weibel et al. proposed to circumvent this issue by using CNTs just over the heated area and a higher permeability material such as sintered copper mesh over the rest of the evaporator wick [101]. Cai and Chen created biporous CNT arrays by patterning the CNT growth on silicon substrates to form various striped and pillar arrays [102]. The biporous CNT structures were able to dissipate up to 600 W/cm^2 over a 2 × 2 mm^2 heated area.

In the majority of the aforementioned studies of capillary-driven evaporation/boiling in porous wicks, biporous and/or hierarchical structures have emerged as higher performance alternatives to their homogeneous counterparts. Depending on the different combinations of length scales considered, however, heterogeneous wicks may not always perform better than homogeneous structures. Ravi et al., for instance, showed that silicon micropillar wicks ($d = 42\ \mu$m, $p = 90\ \mu$m, $h = 100\ \mu$m) capped with a mesh structure to increase the capillary pressure could greatly reduce the dryout heat flux compared to the homogeneous baseline wick if the mesh thickness (1 μm) and pore size (4 μm) were too small [29]. With a sufficiently thick mesh (180 μm) and larger pore openings (15 μm), however, the dryout heat flux could be improved by almost 200% over the baseline. The precision afforded by the vast array of micro/nanomaterials fabrication techniques compatible with silicon substrates creates many promising opportunities for thermofluidic optimization of the heat and mass transport within silicon vapor chambers, though careful design is necessary to ensure performance improvement as opposed to detriment.

5 Packaging Opportunities Enabled by Silicon Vapor Chambers

Successful large-scale production of robust silicon vapor chambers opens up exciting new packaging opportunities for electronics thermal management. Perhaps the simplest compelling use case scenario for a silicon vapor chamber can be envisioned by comparing a traditional microprocessor package with a copper heat spreader, as shown in Fig. 10(*a*), with the various other packaging scenarios enabled by a silicon vapor chamber. As mentioned in the introduction, the thermal interface material between the die and copper spreader, typically referred to as TIM1, must be mechanically compliant to accommodate the CTE mismatch within the package. If the metal lid is replaced by a silicon vapor chamber as shown in Fig. 10(*b*), however, the requirement for mechanical compliance could potentially be relaxed in lieu of lower thermal resistance interfaces with the die. Vadakkan et al. demonstrated through simulation that using a silicon vapor chamber in place of a standard copper lid could reduce the compressive stress in the die by as much as 96% [103]. Eutectic die attach or similar could be utilized to achieve high thermal conductivity, minimal bond line thickness interfaces between the die and vapor chamber [104–106].

Another potential implementation of a silicon vapor chamber could be as shown in Fig. 10(*c*). Solid silicon interposers with through silicon vias (TSVs) are widely accepted as cost-effective methods for creating power-efficient interconnects in multichip packages [107,108]. Though silicon can lead to higher electrical losses compared to organic and glass substrates [109], using an interposer with a higher thermal conductivity can play a significant role in reducing the overall package thermal resistance [110]. Packaging architectures where the heat primarily goes through the substrate may therefore benefit from higher thermal performance interposers such as the one shown in Fig. 10(*c*), where a future interposer could form a self-contained silicon vapor chamber. Choice of a high dielectric strength working fluid would be important to ensure electrical isolation of TSVs that would have to transcend the vapor core, and fabrication would certainly be more challenging than existing solid interposers. As packages become increasingly thermally limited, however, such architectures may be worthwhile considerations.

Finally, yet another packaging opportunity with a silicon vapor chamber could be as shown in Fig. 10(*d*), where evaporative wicking structures are etched directly into the solid substrate of the die. This approach would eliminate any thermal bottlenecks associated with intermediary thermal interface materials, bringing the heat spreading as close to the heat generation sources as possible. A complete vapor chamber could be formed by then bonding a

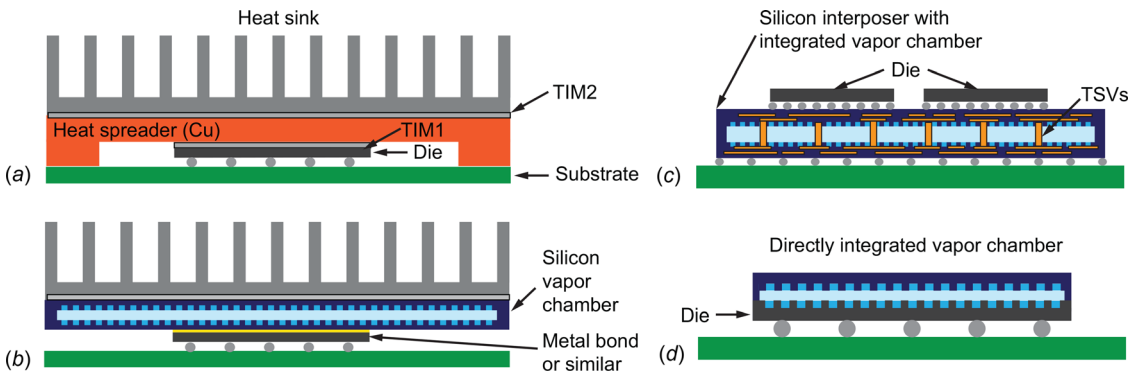


Fig. 10 (*a*) A traditional packaging scheme with a solid copper spreader or copper vapor chamber. (*b*) A potential packaging scheme with a silicon vapor chamber as the heat spreader, where a lower resistance metal bond could be used for die attach. (*c*) Another possible configuration where a future silicon interposer has an integrated vapor chamber to spread heat between multiple die. (*d*) A directly integrated vapor chamber with evaporator wicking structures fabricated directly onto the backside of the die, eliminating the need for any thermal interface layer between the die and spreader.

cap condenser wafer on top of the die. The condenser cap could either be larger than or equal to the die area depending on the heat source areas under consideration. While a larger condenser area equates with more heat spreading area, die-matched, directly integrated vapor chambers will be significantly simpler from a fabrication standpoint, enabling wafer-level matching of condenser cap and device wafers. With that being said, however, there will certainly be a minimum size requirement, below which a vapor chamber will no longer be an effective spreader. What this minimize size is and whether a die-matched vapor chamber will be an effective spreading solution will depend on a number of factors including the hotspot heat flux, heat source to vapor chamber area ratio, and thicknesses of the various substrates involved.

6 Remaining Manufacturing and Application-Level Considerations for Silicon Vapor Chambers

As discussed in the preceding review, silicon vapor chambers with various form factors and wick designs have been demonstrated in literature. The spreading performance of the vapor chambers have been demonstrated to significantly exceed that of benchmark solid silicon spreaders, and various porous wick fabrication strategies are feasible to optimize the maximum heat transfer capacity of the devices. In this section, we will discuss some of the remaining considerations for large-scale adoption of silicon vapor chambers and provide some perspective on the future outlook for this technology.

6.1 Scalability of Manufacturing Approaches. While the manufacturing approaches described in Sec. 3.2 are convenient on a laboratory scale, such filling and evacuation processes may be difficult and impractical for large-scale manufacturing. In a review of early pioneering work on silicon micro heat pipes, Peterson discussed several potential evacuation, charging, and bonding methods for micro heat pipes that could be translated to large-scale, wafer-level silicon vapor chamber production approaches [111]. One proposed method was to place an unsealed micro heat pipe array in a high pressure chamber, evacuate the chamber of NCGs, then fill the chamber with a predetermined amount of working fluid. After heating the chamber above the critical temperature of the fluid, the micro heat pipes could then be sealed while still inside the chamber with an UV bonding process. The final liquid charge volume remaining in each device after charging would be determined based on the volume of the pressure chamber and total amount of introduced working fluid. A similar principle could be applied to the fabrication of silicon vapor chambers to allow for wafer-level evacuation, charging, and sealing. A different bonding process would have to be utilized, however, as UV bonding requires a UV transparent cap wafer.

A promising alternative could be to utilize induction heating as a noninvasive mechanism to seal the vapor chambers while inside a pressurized chamber. Dhillon et al. successfully created hermetic seals for individual silicon micro loop heat pipes by using induction heating to melt solder preforms [112]. The processes involved included metallizing the charging ports, then placing circular solder preform rings on top of each of the devices. Each of the cavities was evacuated and charged with liquid at the individual device level, and localized heating with a heating torch was used to boil off water around the solder preform regions. The solder preforms were then melted around the charging ports with induction heating, resulting in a solder ball that successfully formed a hermetic seal over ports as large as $1 \times 1\,\text{mm}^2$ [112].

Combining this sealing mechanism with the evacuation and charging process proposed by Peterson [111] could potentially be a viable pathway for wafer-level charging and sealing of silicon vapor chambers. As seen in Fig. 11, an ideal process flow could begin with a bonded wafer pair, where evaporator and condenser wafer substrates are first joined together with one of the many dry wafer bonding processes described in Sec. 3. Each individual

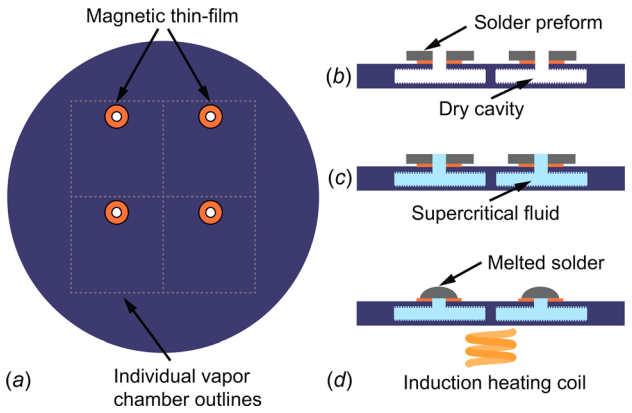


Fig. 11 A proposed wafer level charging and sealing approach for silicon vapor chambers. (*a*) Top view of a dry bonded wafer pair with fill ports metalized with magnetic thin films. (*b*) Cross sectional view of solder preforms placed on top of the fill ports for each vapor chamber cavity. (*c*) After placing the vapor chamber wafer into a pressurized chamber, the chamber and vapor chamber cavities are filled with supercritical working fluid. (*d*) Induction heating melts the solder preforms, sealing the working fluid within each of the vapor chamber cavities.

vapor chamber cavity would require a fill port metalized with a magnetic thin-film similar to that used by Dhillon et al. [112], as shown in Fig. 11(*a*). After placing solder preforms on top of each fill port (Fig. 11(*b*)), the bonded wafer pair would then be placed into a high pressure chamber. Following the process described by Peterson [111], the chamber would be evacuated of NCGs and filled with working fluid heated above the critical point. As shown in Fig. 11(*c*), the supercritical fluid would enter the vapor chamber cavities through the open fill ports. Melting the solder preforms with induction heating would then hermetically seal the cavities, containing the fluid within (Fig. 11(*d*)). One potential challenge with this approach would be finding an ultrahigh temperature sealing solder with a melting point above the critical temperature of the working fluid. For water, this would require a solder with melting point above 374 °C and chemical compatibility with the remaining silicon vapor chamber components.

6.2 Maximum Temperature Limitations. The maximum temperature of heat pipes and vapor chambers is typically limited by two factors: an undesirable change in fluid properties as the temperature approaches the critical point of the fluid, or mechanical failure due to stress generation in the vapor chamber walls as the vapor temperature (and internal pressure) increases. With water as the working fluid, the maximum operating temperature of silicon vapor chambers tends to be limited by the latter. Cai et al. found through simulation that mechanical support pillars between the evaporator and condenser surfaces were necessary to prevent bursting of the silicon walls above approximately 180 °C for a $3\text{x}3\,\text{cm}^2$ vapor chamber [45]. The authors observed that the highest stress regions occurred at the edges of the vapor cavity, and arranging a number of support pillars in a diamond configuration throughout the cavity could help with the stress distribution. They did not account for the bonding interface used between the evaporator and condenser surfaces, however, which could present another failure mechanism [113]. While 180 °C is above the typical maximum operating temperature of silicon electronic devices (120 °C), a silicon vapor chamber attached to or integrated with silicon electronics may still need to survive higher temperatures during various other packaging processes such as die attach and/or solder reflow. Power electronics devices utilizing wide bandgap semiconductors such as GaN and SiC also frequently operate at 200 °C or above [114]. The maximum operating temperature due to burst pressure limitations is therefore an important consideration when assessing whether or not silicon vapor chambers are

suitable for various electronic packages. Mechanical limitations may also create constraints for bonding, evacuation, and liquid charging procedures. Since the silicon vapor chambers investigated in literature thus far have been bonded under dry conditions, high temperature bonding processes such as glass frit and eutectic can be tolerated without any mechanical limitations. If bonding were to occur in a wet environment, however, the mechanically constrained maximum operating temperature of the vapor chamber could impact the bonding temperature, unless the required heating for bonding could be appropriately localized to the bonding areas only.

Overall, the mechanical properties of silicon vapor chambers have not been extensively studied. This remains an important area for further investigation, as the mechanically limited maximum operating temperature of silicon vapor chambers will play a large role in determining how these devices can be utilized and manufactured. Future research in this area may benefit from techniques leveraged in piezoresistive silicon pressure sensor fabrication, where rounding of etched cavity edges, etc., have been demonstrated as effective methods to reduce stress concentrations at sharp corners [115].

6.3 Benchmarking With Other Technologies. Thus far, the performance of silicon vapor chambers has primarily been compared to solid silicon as a reference benchmark. In this section, we will explore other materials with similar CTE values that could also potentially be used to form vapor chambers. For silicon vapor chambers to emerge as viable candidates for widespread use in electronic packages, there must be a clear performance and cost benefit compared to other competing technologies.

Titanium is one such alternative material that has been investigated for vapor chamber applications due to its relatively lower CTE compared to other metals (8.5 ppm/K [116]) and high-tensile strength [117]. Ding et al. developed a 0.6 mm thick, 3x3 cm^2 vapor chamber fabricated from titanium substrates with etched titanium pillars as the evaporator wick [118]. The vapor chamber was estimated to have a maximum effective thermal conductivity of approximately 350 $Wm^{-1}K^{-1}$ with a hot side operating temperature of 105 °C. Copper molybdenum (CuMo) or copper tungsten (CuW) alloys have also frequently been used as lower CTE heat spreaders for electronics thermal management. Altman et al. explored the use of CuMo/Cu laminate sheets to form a 3 mm thick, 3x3 cm^2 vapor chamber with sintered copper particle wicks [119,120]. The vapor chamber was able to reduce the device to ambient thermal resistance by up to 26% relative to a solid CuMo spreader [120]. Hose et al. utilized a similar fabrication approach to create a vapor chamber with a CuW envelope and demonstrated a 43 °C reduction in junction temperature compared to solid CuMo [121]. Additional low CTE materials that have been explored for use in vapor chamber and heat pipe applications also include aluminum nitride [122] and Kovar [123].

Vapor chambers formed from low CTE metal alloys such as CuMo and CuW may perhaps pose the largest source of competition to silicon vapor chambers. While titanium is an appealing vapor chamber material due to its high structural strength, widespread usage may be prohibited by the high inherent material cost. CuMo/CuW, on the other hand, have solid thermal conductivities comparable to Si and can be processed with very low cost technologies such as sheet-level stamping, while the area cost scaling of silicon vapor chambers is limited by the current 12 inch industry wafer size. In addition to cost, however, package architecture will also play a large role in determining which type of vapor chamber may be most suitable for future applications. The CTE of CuMo/CuW is still relatively high compared to most semiconductors, making a CuMo/CuW vapor chamber nonideal compared to a silicon vapor chamber for bonding to and cooling from a bare die. CuMo/CuW vapor chambers could be better suited, however, for power modules where the spreader is typically attached to an intermediary direct bond copper (DBC) laminate [124] instead of directly to the die.

Perhaps the most compelling use case for silicon vapor chambers then remains in the possibility of direct integration with semiconductor dies, where evaporative wicking structures can be formed directly into the die substrate. This type of packaging scenario is uniquely accessible to silicon vapor chambers, which can be streamlined into the same process flows as the semiconductor chips. There is also opportunity for integrated silicon vapor chambers to be combined with embedded microchannel cooling for thermal management of high heat flux chips, potentially acting as a replacement for costly diamond films that have been used previously for intermediary heat spreading [11]. Whether or not the silicon vapor chamber spreading performance can approach that of a diamond film, however, will require careful consideration on a case-by-case basis depending on the overall spreading area and heat fluxes involved. Vapor chambers with various envelope materials have been characterized in many situations to have effective thermal conductivities exceeding that of diamond [125], but it is erroneous to assume that vapor chambers will always perform better. As the high effective thermal conductivity portion of the vapor chamber is confined to the vapor cavity region, smaller area vapor chambers will suffer in terms of relative performance compared to solid spreader equivalents.

7 Concluding Remarks

A number of experimental studies in literature have demonstrated successful laboratory scale fabrication, evacuation, liquid charging, and thermal characterization of silicon vapor chambers with various form factors and wick structures. While the physical phenomena governing silicon vapor chamber operation have been studied for decades, the use of silicon as a vapor chamber envelope material introduces challenges and opportunities that may impact their feasibility for mitigating hotspots as part of future thermal management systems.

One challenge is scalability of dimensions. Of potential concern is that existing liquid charging and NCG evacuation processes have all been performed at the individual device-level as opposed to wafer-level. Smaller silicon vapor chambers designed for die-level heat spreading also require high amounts of liquid charging precision, creating strict guidelines for future process development strategies. While well-established methods exist for high volume evacuation, filling, and sealing of individual metal-based vapor chambers, such operations involving welding and crimping of metal charging tubes may be difficult to integrate with semiconductor manufacturing foundries that would likely be utilized to manufacture silicon vapor chambers. The overall mechanical reliability of silicon vapor chambers is also an area that warrants further investigation, as the maximum operating temperature due to burst pressure limitations could limit packaging opportunities for silicon vapor chambers.

Since silicon is CTE matched to most semiconductor substrates, the use of a silicon vapor chamber enables a variety of new packaging configurations, such as high thermal performance metal bonding between the die and the vapor chamber or direct integration of evaporative wicking structures into the die substrate. The precision and flexibility enabled by MEMS silicon micromachining processes has also led to the development of various biporous and/or hierarchical structures that can be fabricated on top of silicon substrates for optimized thermofluidic performance as vapor chamber wicks. If the previously mentioned challenges of mechanical reliability and manufacturing scalability can be addressed, silicon vapor chambers may be promising options for hotspot management in future high heat flux electronic devices.

Acknowledgment

T. Liu acknowledges support from the NSF Graduate Research Fellowship Program. The authors also acknowledge support on

this topic from Analog Devices, Inc. and the National Science Foundation Engineering Research Center for Power Optimization of Electro-Thermal Systems (POETS) with cooperative agreement EEC-1449548. Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the National Science Foundation.

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