Two-Fold Reduction of Switching Current Density in Phase Change Memory Using Bi_2Te_3 Thermoelectric Interfacial Layer

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***Abstract*— High switching current density has been a key bottleneck for phase change memory (PCM) technology. Here, we demonstrate interfacial thermoelectric heating (TEH) as a promising way of tackling this challenge. We use TEH induced by a thin Bi_2Te_3 interfacial layer to demonstrate ∼2× reduction of reset current density (J_{reset}) and power (P_{reset}) compared to control PCM devices based on $Ge_2Sb_2Te_5$ (GST). Measurements of polarity-dependent reset current and power in well-cycled devices reveal the strong TEH caused by the Bi_2Te_3 interfacial layer. The TEH origin of J_{reset} reduction is further confirmed by electro-thermal simulations. Such TEH-engineered PCM devices are scalable with the bottom electrode diameter and thus could be promising for high density data storage applications.**

***Index Terms*— Phase change memory, interfacial thermoelectric engineering, reset current density reduction.**

I. Introduction

PHASE change memory has shown promise for storage-class applications due its fast switching speed, good resistance window, and scalability [1], [2]. PCM also offers nonvolatility and longer write endurance than flash memory [1], [2]. However, concerns remain over its relatively high reset current density (J_{reset}) and power (P_{reset}), both for data storage and emerging applications such as neuromorphic computing [1]–[3]. In addition, the reset current (I_{reset}) of PCM must be provided by selector devices in a memory array. As a result, the selectors need to have larger area, limiting storage density [1], [4]. Hence, reduction of J_{reset} is essential for high density data storage [2], [5]. In a PCM cell, data are encoded as the resistance change of a phase change material (like $Ge_2Sb_2Te_5$, or GST) contacted by a top and bottom electrode (BE). Resistive heating induced by the BE can reversibly transform the GST between amorphous (high-resistance) and crystalline (low-resistance) states. Reducing the BE diameter reduces I_{reset}, but J_{reset} does not decrease unless the heating efficiency is improved [2], [4], [6].

Heating efficiency could be improved with better thermal insulation of the PCM cell [7], [8], or by improving the heating process itself. Commonly, the latter only relies on Joule heating, however thermoelectric heating (TEH) could also be introduced, especially because GST itself has a non-negligible, positive Seebeck coefficient (S_p) [9], [10]. Hence, utilization and enhancement of this TEH effect can decrease the requirement of large J_{reset} in PCM [10]. Several previous studies have modeled and characterized TEH in GST [10]–[12]. Also, by using a polysilicon BE instead of a TiN BE, a moderate ∼25% reduction of I_{reset} has been experimentally demonstrated due to TEH [13], further inspiring such work.

Here we show a ∼2× reduction of J_{reset} in mushroom-cell PCM with TEH induced by a thin Bi_2Te_3 interfacial layer at the BE interface. Bi_2Te_3 is a thermoelectric material with significant but negative S_n [14]–[16], which amplifies the TEH effect at the Bi_2Te_3/GST interface due to the difference in their Seebeck coefficients, thus improving the overall heating efficiency. Polarity-dependent experiments and simulations further confirm the TEH effect arising from interfacial engineering to reduce J_{reset} and P_{reset} at similar voltage, while maintaining scalability with the BE diameter.

II. Device Fabrication and Measurement

Figs. 1(a,b) show the schematic and the cross-sectional scanning electron microscope (SEM) images of our Bi_2Te_3/GST PCM devices with ∼4 nm Bi_2Te_3 and ∼50 nm GST thickness, here on a ∼150 nm diameter TiN BE. Before sputter depositing ∼4 nm polycrystalline Bi_2Te_3 at room temperature (RT), we clean the BE surface *in situ* with Ar ions to remove native TiO_x [8], then we anneal at 180°C for 30 minutes. We subsequently sputter 50 nm GST and then ∼10 nm TiN capping layer at RT, all without breaking vacuum. Next, we pattern and dry etch the device region followed by the fabrication of top electrode (TiN/Pt) using sputtering. For set and reset programming, we use 1/20/300 ns and 1/20/1 ns rise/width/fall pulses, respectively,

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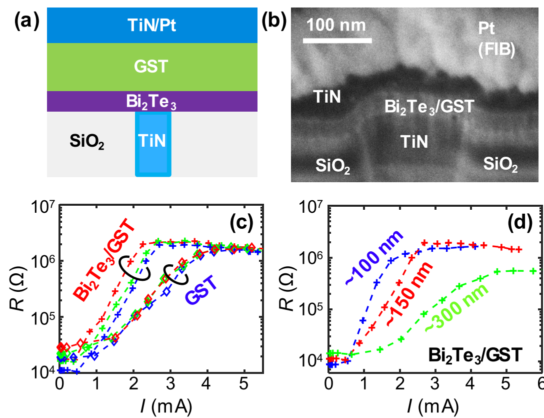

Fig. 1. Device Structure and Electrical Measurement: (a) Schematic of the PCM device with 4 nm thin Bi_2Te_3 layer and 50 nm GST. (b) SEM cross-section of a fabricated device. Read resistance vs. current (c) for multiple devices (with ~150 nm BE diameter) showing the reset current (I_{reset}) reduction when Bi_2Te_3 layer is present. (d) I_{reset} reduction with BE diameter in Bi_2Te_3/GST.

and measurement details were further described in [8]. Unless stated otherwise, all measurements reported here were done after cycling the devices 3000 times to ensure reliable and consistent operation.

III. Results and Discussion

Fig. 1(c) displays resistance (R) vs. current (I) for multiple devices with ~150 nm BE diameter, showing ~2× lower I_{reset} for Bi_2Te_3/GST vs. control GST devices. Fig. 1(d) shows I_{reset} of our devices scales with the BE diameter (here from ~100 to ~300 nm), demonstrating the scalability [4] of this technology.

Examining the reset current density in Fig. 2(a) reveals that J_{reset} for our mushroom-type Bi_2Te_3/GST is ~10 MA/cm^2, half that of a control GST device (~20 MA/cm^2, typical for GST in this configuration [4], [8]). Figs. 2(b,c) show Bi_2Te_3/GST devices switch at similar voltage and thus ~2× lower P_{reset} compared to GST control devices. Fig. 2(d) reveals that Bi_2Te_3/GST devices can maintain ≥10× resistance ratio for ≥10^5 cycles. Fig. 2(e) shows the stability of the Bi_2Te_3/GST devices, as the ~2× reduction in I_{reset} is maintained even after 10^4 switching cycles. We also find ~40% less resistance drift (υ = resistance drift coefficient) compared to control GST PCM devices [Fig. 2(f)], thereby projecting larger retention in the Bi_2Te_3/GST devices.

Next, we perform polarity dependent measurements (NP = normal polarity, RP = reverse polarity) with Bi_2Te_3/GST and control GST devices, as shown in Figs. 3(a,b). While Joule heating is always positive, the thermoelectric effect is expected to switch sign when the current direction is reversed *i.e.* from TEH in NP to cooling in RP [10]. As shown in Fig. 3(c), Bi_2Te_3/GST devices require ~2× lower I_{reset} in NP vs. RP operation, a direct consequence of the thermoelectric effect at the Bi_2Te_3 (n-type) to GST (p-type) interface. Crystalline GST has $S_p > 0$ (≈ 40 to 100 μV/K from RT to 200°C) [9], [10], [13], whereas Bi_2Te_3 films have large $S_n < 0$ (≈ -200 μV/K to -150 μV/K from RT to 200°C) [15]. The sign of the Seebeck coefficient indicates if the charge current flows in the same or opposite direction as the heat carried by holes or electrons, respectively. In addition, it is the *difference* in Seebeck coefficient ($\Delta S = S_p - S_n$) which drives an interfacial thermoelectric heating or cooling effect [10], [17]. $|S_n|$ is expected to increase for thinner layers

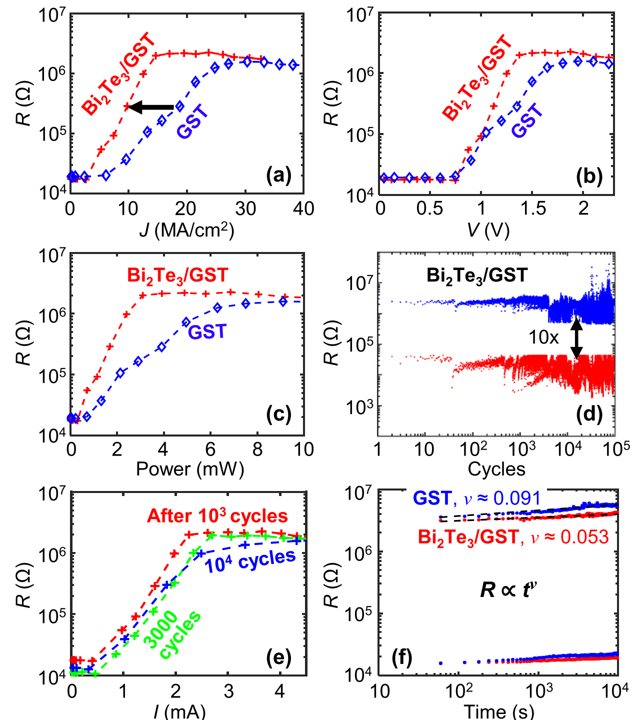

Fig. 2. Electrical Analysis: Measured DC resistance vs. reset (a) current density, (b) voltage, (c) power for PCM devices with and without Bi_2Te_3 interfacial layer (all with ~150 nm BE diameter). J_{reset} and P_{reset} are reduced by ~2× for Bi_2Te_3/GST devices. (d) Over 10× resistance ratio maintained for 10^5 cycles in Bi_2Te_3/GST devices. (e) Read resistance vs. current after many switching cycles in a Bi_2Te_3/GST device (~150 nm BE diameter), showing that the ~2× lower I_{reset} is preserved. (f) Resistance drift (v is the drift coefficient extracted from the fitted dashed black lines using $R \propto t^v$ where t is time) comparison for PCM devices with (red) and without Bi_2Te_3 interfacial layer (blue).

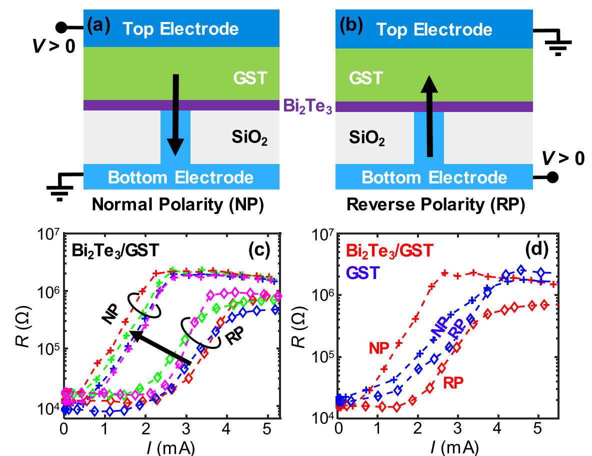

Fig. 3. Polarity-dependent electrical measurement: Schematic showing (a) normal polarity (NP) and (b) reverse polarity (RP). (c) Read resistance vs. current for Bi_2Te_3/GST device operated in NP and RP for multiple cycles. (d) Resistance vs. current for Bi_2Te_3/GST (red curves) and GST (blue curves) devices operated in NP and RP, showing the strong TEH due to the inclusion of the thin Bi_2Te_3 interfacial layer.

like Bi_2Te_3(~4 nm here) [18] due to carrier confinement [16], [19], further enhancing ΔS at the interface.

In contrast, control GST devices in Fig. 3(d) display only small intrinsic asymmetry with respect to the current flow direction [10], confirming the much larger TEH introduced by the thin Bi_2Te_3 layer in Bi_2Te_3/GST devices. At the same time, we note that the Bi_2Te_3 layer only introduces ~13%

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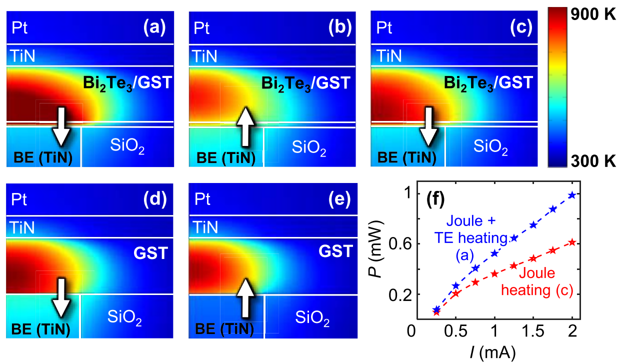

Fig. 4. Electro-thermal simulations: Temperature distribution in our PCM devices with and without Bi_2Te_3 layer, at the end of a current pulse (2 mA, 20 ns). (a) NP with 4 nm Bi_2Te_3 and 50 nm GST layer. (b) RP for the same. (c) NP for the same, but assuming no thermoelectric effect in the Bi_2Te_3 ($S_n = 0$). (d) NP for GST-only (50 nm) PCM device and (e) RP for the same. White arrows show the direction of current flow. All simulations have BE (TiN) diameter of 150 nm and the axis of cylindrical symmetry is the left edge of the simulation domain. (f) Heating power for the configuration in (a) shows ~60% contribution of thermoelectric heating at the end of a NP current pulse, compared to (c).

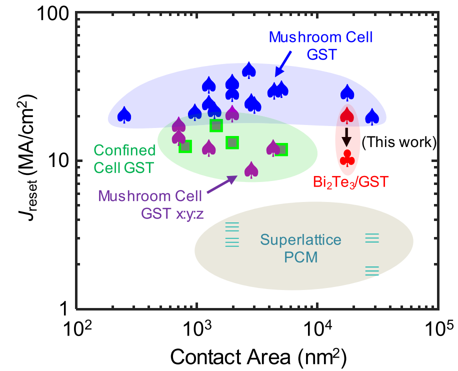

Fig. 5. Benchmarking: Measured reset current density (J_{reset}) vs. contact area for various PCM technologies. Results from this work are shown in red, for our mushroom cells with Bi_2Te_3/GST and control GST. J_{reset} for other PCM devices in the literature are obtained from Refs. [1], [4], [7], [8], [13], [26]–[34], [37]. "GST" refers to the 2:2:5 stoichiometry, except where noted with "*x:y:z*".

additional thermal resistance in the PCM stack, as shown by separate thermal [20] measurements on similar blanket films (**Dataport Fig. S1** at DOI: 10.21227/wq7q-bx17). In other words, the small additional thermal resistance alone cannot be responsible for the ~2× change in J_{reset}, instead pointing to the key role of TEH at the Bi_2Te_3/GST interface.

To gain deeper insight, we perform finite element electro-thermal simulations of the device structures from Figs. 3(a,b), including both Joule heating and thermoelectric phenomena. This approach solves the heat equation self-consistently with the current flow [10], taking advantage of the cylindrical symmetry of the PCM device (Fig. 4). The Seebeck heating or cooling is $IT\Delta S$ at the junction of two materials, e.g. between GST and Bi_2Te_3, between Bi_2Te_3 and TiN, or between GST and TiN. These simulations also include the T-dependent thermal conductivity, resistivity, and S_p of GST [12], [13], [21], [22], T-dependent S_n of Bi_2Te_3 [15] and of TiN [12], T dependent thermal conductivity and electrical resistivity of TiN and Bi_2Te_3 [23]–[25] as well as the measured thermal and thermal boundary resistances at the appropriate interfaces.

Fig. 4 shows the temperature profiles computed in the Bi_2Te_3/GST and GST PCM at the end of a reset pulse (2 mA, 20 ns) for both NP and RP. In NP operation, the Seebeck effect generates additional TEH, due to the positive ΔS between GST and Bi_2Te_3. This helps the GST reach the melting temperature at lower I_{reset}. TEH causes a significantly altered temperature distribution between NP and RP in a Bi_2Te_3/GST device [Figs. 4(a,b)] compared to a control PCM device [Figs. 4(d,e)]. If the thermoelectric effect is ignored in the Bi_2Te_3 layer, the NP temperature profile closely resembles that of the GST-only device, as shown in Figs. 4(c,d). In Fig. 4(f) we also plot the total heating power at the end of a NP current pulse for our Bi_2Te_3/GST devices, revealing TEH adds significantly (~60%) to the Joule heating component when it is included in simulations.

Our PCM technology with enhanced TEH and reduced P_{reset} could be promising for high density data storage applications. As shown through benchmarking in Fig. 5, our Bi_2Te_3/GST mushroom PCM cells have ~2× lower J_{reset} (~10 MA/cm^2) compared to similar GST mushroom cells (with 2:2:5 stoichiometry) from the literature [7], [8], [26]–[29] including control GST devices (~20 MA/cm^2) in this study. We note that lower J_{reset} *could* be achieved with different stoichiometries (x: y: z) or doping of GST in mushroom cells (purple symbols in Fig. 5). However this comes at the expense of higher (10× to 100×) resistivity and switching voltage vs. traditional GST 2:2:5 [30], [31], negating part of the improvement in P_{reset}. In contrast, our Bi_2Te_3/GST cell does not increase the switching voltage and low-resistance state (Fig. 2), and the ultrathin Bi_2Te_3 layer could also be combined with other stoichiometries of GST (x: y: z).

Lower J_{reset} could also be achieved by structural (e.g., pore or edge type geometry) [1], [4], [13], [32] or by electro-thermal confinement in superlattice heterostructures [28], [33], [34]. This, however, often comes with added fabrication complexity and cost. However, our TEH-engineered PCM could also be combined with confinement to achieve further J_{reset} reduction [**Dataport Fig. S2** at DOI: 10.21227/wq7q-bx17]. Additional reduction in I_{reset} and P_{reset} could be achieved by optimizing the interfacial thermoelectric layer with larger negative S_n (e.g., Bi_2Te_3-Sb_2Te_3 alloys with 70% Bi content [35], Bi-doped SnSe ($Sn_{0.94}Bi_{0.06}Se$) [36]), enhancing the TEH at the interface with the phase change material. Further material characterization and imaging of the thermoelectric interface will also provide useful insight into the optimization of such PCM in terms of thermal stability and device failure mechanism.

IV. Conclusion

We introduced a novel, thermoelectrically-enhanced PCM with a thin Bi_2Te_3 interfacial layer in an otherwise common mushroom-cell configuration. Such devices achieve ~2× reduction in reset current density due to the additional thermo-electric heating caused by the Bi_2Te_3 layer. Devices display scalability with BE diameter, and could be combined with other PCM options (e.g. structural or thermal confinement) to further reduce the reset current density. These results should inspire further studies of thermoelectric heating as a novel pathway for low-power high-density PCM data storage.

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