# Next Generation Gallium Nitride HEMTs Enabled by Diamond Substrates

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*Abstract*— **This paper describes the thermal and electrical performance of GaN on Diamond devices, where the GaN on Diamond substrates are fabricated by taking epi from a host growth substrate and replacing it through direct growth of CVD diamond. We have found GaN on Diamond material improves thermal performance while maintaining electrical performance. This work demonstrates that GaN on Diamond technology can form the foundation of a next generation GaN device with 3X (or more) higher areal power density.**

*Keywords—GaN, diamond, HEMT, thermal interface resistance*

## I. INTRODUCTION

Gallium Nitride technology has emerged from research and development and is now being inserted into next generation RF electronic systems [1]. Its higher bandgap and operating voltage enables higher power densities than the incumbent GaAs technology, resulting in improved performance and $/Watt cost savings. It has become very clear that in some system applications, GaN device power dissipation must be restrained in order to limit peak device junction temperatures and maintain reliability. Reducing temperature rise with on-chip thermal management would enable increased power density, enabling a new wave of next generation GaN transistors. This paper summarizes thermal and RF device results achieved by replacing GaN epi's growth substrate with CVD diamond.

## II. GaN ON DIAMOND WAFER FABRICATION AND PERFORMANCE

GaN on Diamond wafers were created by Group4 Labs [2], now Element 6 [3]. The original GaN growth substrate was removed and replaced with diamond through a direct growth process (Figure 1). We produced GaN on Diamond wafers with approximately 100μm of substrate thickness, varying in diameter from 1 inch to 3 inch. Their sheet resistance ranged from 465 to 670 Ohms/square, with the best wafer approaching the typical GaN on SiC sheet resistance of ~410 Ohms/square. The epi did experience some damage during the transfer to
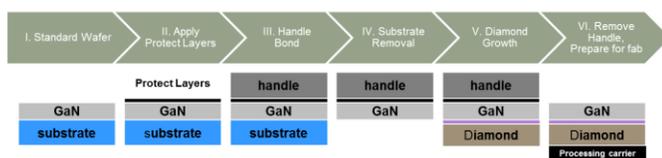


Figure 1: Process flow for creating GaN on Diamond wafers

diamond. Typical defects included epitaxial voids due to imperfect handle bond and epi surface pitting due to defects and surface contamination during the protect layer process. We characterized the transferred GaN epi with standard wafer characterization measurements such as C-V. Results showed epi with a sharp transition from the off to on state and no sharp, pronounced charge deep in the GaN buffer, which would be indicative of buried charge. These measurements suggest the GaN epi is intact after the handle and diamond growth process steps and can support fabrication of GaN transistors.

## III. GaN ON DIAMOND DEVICE RESULTS

### A. Device Fabrication

Devices were fabricated on two wafers in Raytheon's foundry, located in Andover, MA. Wafer 1 was a 1-inch wafer with only 50% epi visual yield but still had 10 transistors that completed all DC and RF characterization tests. Wafer 2 was a 3-inch wafer with higher epi yield (Figure 2). This subsequent wafer featured over 300 functional transistors.
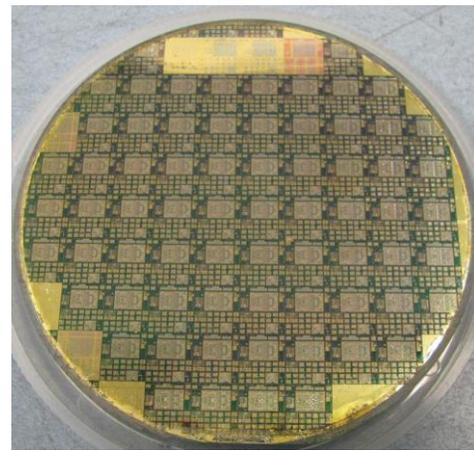


Figure 2: 3-inch GaN on Diamond wafer after completion of fabrication

### B. Electrical Characterization

Electrical characterization included industry-standard DC I-V tests that measured leakage, transconductance, and saturated current ($I_{max}$) of the transistor. Our test vehicle transistor was a 10x125μm transistor, which has 10 gate fingers, each 125μm in width, for a total of 1.25mm of

transistor periphery. The GaN on SiC baseline transistor has gate fingers spaced 40µm apart. The GaN on Diamond transistors have the same periphery but with gate pitch of 40, 30, 13, and 10µm. The smaller gate pitches take advantage of the better thermal performance and increased power per area (W/mm$^2$) (Figure 3). DC test was followed by small-signal RF test. GaN on Diamond devices exhibited lower $I_{max}$ and small-signal gain than our standard devices, as well as higher gate leakage [4]. However, this performance was expected given the higher sheet resistance measured during wafer characterization. The best performing devices were then subjected to RF loadpull testing. This test measures the power and efficiency of the transistor under large-signal compressed operation. We used a Maury Microwave loadpull bench operating at 10 GHz with all devices tested at 28V operation. Devices were measured at the fundamental load matched for an optimum balance between output power and PAE, corresponding to Class-AB operation. Harmonic impedances were measured but not controlled.
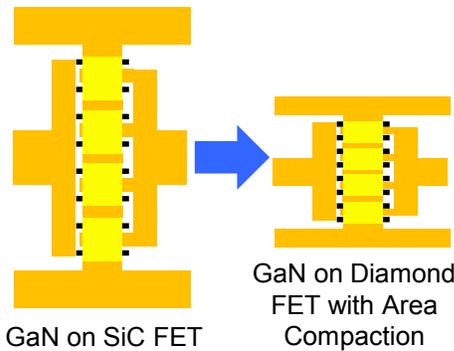


Figure 3: Example HEMT area reduction due to compaction of gate to gate spacing

Measurements were taken on Wafer 1 and Wafer 2 as well as a GaN on SiC wafer as a baseline comparison to state of the art (Figure 4 and 5). The GaN on SiC transistor's baseline performance was measured to be 5.50 W/mm of RF output power with PAE of 61.5%, as shown in the top row of both tables. Devices of identical geometry on Wafer 1 with lower epi performance measured 3.10 and 3.95 W/mm with 25.8 and 37.9% PAE. Devices with 30µm gate pitch measured 3.63 and 4.17 W/mm and 30.0 and 39.3% PAE. Wafer 1 yielded one device with 10µm gate pitch, which measured 3.71 W/mm and 33.5% PAE. This device has a 4X reduction in transistor area relative to our baseline device, which is a 2.70X increase in areal power density (W/mm$^2$) relative to state of the art GaN on SiC performance.

| Type | G2G | POW (W/mm) | Pout (W/mm$^2$) Relative to SoA | PAE (%) |
|---|---|---|---|---|
| Prod. SiC | 40 | 5.50 | 1.00 | 61.5 |
| Diamond | 40 | 3.10 | 0.56 | 25.8 |
| Diamond | 40 | 3.95 | 0.72 | 37.9 |
| Diamond | 30 | 3.63 | 0.88 | 30.0 |
| Diamond | 30 | 4.17 | 1.01 | 39.3 |
| Diamond | 10 | 3.71 | 2.70 | 33.5 |

Figure 4: Comparison of RF loadpull performance for GaN on Diamond Wafer 1 transistors relative to GaN on SiC shows a 2.7X increase in areal power density

Wafer 2 produced devices with higher performance due to higher performance epi and implementation of lessons learned during fabrication of Wafer 1. Devices with 40µm gate pitch measured 5.49 and 5.85 W/mm and ~50% PAE. Note that the 5.85 W/mm result is actually higher than the baseline GaN on SiC performance. Devices with 4X compaction due to 10µm gate pitch measured 5.01 – 5.32 W/mm and 51.4 – 56.6% PAE for a 3.65 – 3.87X increase in areal power density (W/mm$^2$). Thus, these devices surpassed the 3X goal of the DARPA NJTT program.

| Type | G2G | POW (W/mm) | Pout (W/mm$^2$) Relative to SoA | PAE (%) |
|---|---|---|---|---|
| Prod. SiC | 40 | 5.50 | 1.00 | 61.5 |
| Diamond | 40 | 5.85 | 1.06 | 49.9 |
| Diamond | 40 | 5.49 | 1.00 | 50.4 |
| Diamond | 10 | 5.32 | 3.87 | 51.4 |
| Diamond | 10 | 5.09 | 3.70 | 55.7 |
| Diamond | 10 | 5.05 | 3.68 | 56.6 |
| Diamond | 10 | 5.03 | 3.66 | 55.1 |
| Diamond | 10 | 5.01 | 3.65 | 55.2 |

Figure 5: Comparison of RF loadpull performance for GaN on Diamond Wafer 2 transistors relative to GaN on SiC shows a 3.87X increase in areal power density

Baseline GaN on SiC and GaN on Diamond devices from Wafer 2 were also sent to AFRL for independent confirmation of RF loadpull results. Relative to Raytheon's measurements, AFRL measured slightly lower power on both the GaN on SiC and GaN on Diamond devices (Figure 5). This difference is attributed to known differences in loadpull benches including available source and load match conditions and harmonic termination. However, AFRL did measure similar relative performance (3.6X increase in areal power density), validating the results measured by Raytheon, with GaN on Diamond devices providing a >3X increase in transistor areal power density.

| Pout @ Peak PAE | GaN/SiC | GaN/DIA |
|---|---|---|
| dBm | 37.69 | 37.22 |
| W | 5.87 | 5.28 |
| W/mm | 4.70 | 4.22 |
| W/mm$^2$ relative to GaN/SiC | 1 | 3.6 |

Figure 5: AFRL measured loadpull results compare favorably with Raytheon measurements, with a 3.6X increase in areal power density for GaN on Diamond

## C. Thermal Characterization

Thermal characterization commenced after completion of electrical characterization. Through Time-Domain Thermo-Reflectance (TDTR), gate thermometry, and Micro-Raman measurements, we systematically verified robust thermal models for GaN on SiC and GaN on Diamond transistors and confirmed simulated results with independent measurements. This process is discussed in detail in prior papers [5,6]. With confidence established in the device thermal models, we used them to compare model-predicted peak junction temperature, defined as the peak nodal temperature that occurs in the model with adequate mesh density. This is useful as the model removes any variations in device type, geometry, and operating condition and permits us to make a direct performance comparison. We employed the models to predict peak junction temperature and provide a comparative assessment of the Wafer 1 and GaN on SiC transistors at a nominal dissipation of $P_{diss}$ = 4.2W/mm (Figure 6). For 40μm gate pitch (40μm gate to gate (g-g) spacing) transistors, the GaN on Diamond device was determined to exhibit a peak junction temperature of 90.3°C, which is 8.5°C (9%) lower than GaN on SiC. The GaN on Diamond HEMT device with 10μm gate pitch was determined to exhibit a peak junction temperature of 113.8°C, which is only 6.3°C (6%) higher than the 30μm gate pitch GaN on SiC transistor but at 3X the dissipation density. As can be seen the benefit provided by GaN on Diamond stems directly from the reduced temperature rise in the device substrate, which is partially offset by increased temperature drop across the GaN-substrate interface (thermal interface resistance - TIR) and packaging. The TIR is associated with the layers between the GaN and the diamond, including heterogeneous interface resistances, and conductivity gradients in the near-nucleation CVD diamond. The temperature drop across the packaging layers is larger in the GaN on Diamond devices due to the increased heat flux presented to the packaging. This is the result of both reduced spreading in the thinner diamond substrate and higher transistor heat flux (for the 10μm gate pitch device). Variations in GaN temperature drop are driven primarily by GaN thickness, with the GaN on Diamond devices featuring a ~0.4μm thinner GaN layer relative to the GaN on SiC devices. Modeling of a GaN on SiC device with 10μm gate pitch indicates that the peak junction temperature would increase 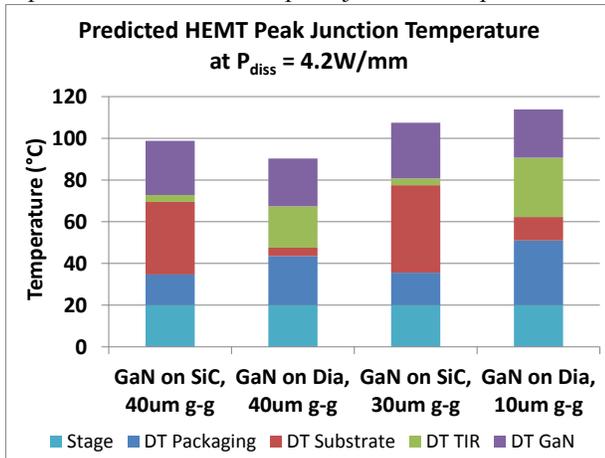more than 50°C relative to a 30μm gate to gate device. This result underscores the importance of the only 6.3°C temperature increase observed in the GaN on Diamond devices for a 3X (from 140 to 420W/mm²) increase in areal dissipation density, as well as the importance of the high conductivity diamond substrate at high transistor areal power density.

A similar analysis was conducted to compare GaN on SiC devices with GaN on Diamond Wafer 1 devices (with 47.6 m²K/GW TIR), and GaN on Diamond Wafer 2 devices (with an improved TIR of 29 m²K/GW [6]). We use the same model to remove all variations between tests (such as layout and packaging differences) to permit a direct comparison of thermal performance related to GaN on Diamond transistors. At 3X the RF output power density, Wafer 1 devices have slightly higher temperatures than the SiC baseline devices (Figure 7). With the improvements in TIR, the Wafer 2 devices have lower temperatures than the baseline, while simultaneously achieving 3X the RF output power density.
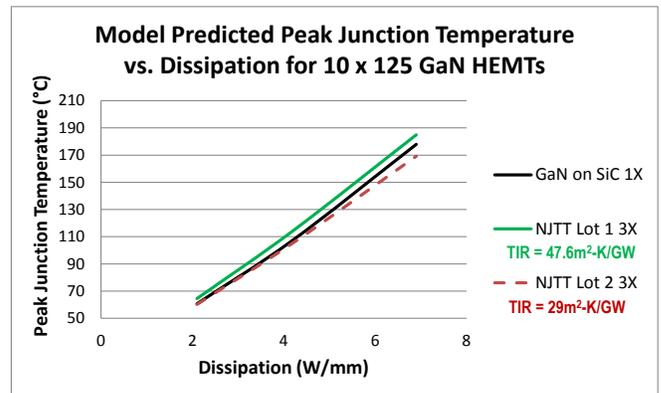


Figure 7: Predicted junction temperature vs. dissipation using validated GaN/SiC, GaN/Diamond Wafer 1, and GaN/Diamond Wafer 2 device models.

## IV. CONCLUSION

Measured electrical and thermal performance of GaN on Diamond transistors indicates that GaN on Diamond technology has the ability to significantly increase transistor power density over current state of the art GaN on SiC, without increasing operating temperature which translates into cost, size, weight, and power advantages for RF systems. Measured electrical performance demonstrated a 3.87X increase in areal power density (W/mm²), surpassing the 3X goal. Strong agreement between gate thermometry, Micro-Raman measurements, and thermal modeling enabled us to demonstrate achievement of a >3X reduction in thermal resistance for a GaN on Diamond transistor. Further development will mature the technology to improve GaN on Diamond epi performance to more closely match that of current GaN on SiC in production today. This improved epi will result in improved transistor performance and further validate the potential for this technology.



Figure 6: Model-predicted peak junction temperatures of GaN on SiC and "Lot 1" Diamond transistors

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