Thermal Characterization of Nanostructured Superlattices of TiN/TaN: Applications as Electrodes in Phase Change Memory

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ABSTRACT

Phase Change Memory (PCM) technology relies on the contrast in electrical resistance between the amorphous and crystalline states of a chalcogenide active material. Electrical PCM devices use Joule heating by short pulses of current to induce phase change, such that the amount of heat injected into the active material and the rate of cooling determine the final state of material formed. In this paper, we explore the possibility of replacing commonly used TiN electrodes by nanostructured superlattices of TiN/TaN that have lower through-plane thermal conductivity, in order to improve the confinement of heat within the phase change material and achieve a reduction in the device programming current. TiN(*m*)/TaN(*n*) superlattices were grown on Si substrates using physical vapor deposition, *m* and *n* representing the intra-period thicknesses of TiN and TaN layers respectively (*m*, *n*: 5 - 25 nm). The through-plane thermal conductivity of these superlattices was measured using time-domain thermoreflectance (TDTR), and was found to be in the range 1.5 – 2 W/m-K, a reduction from the bulk conductivity of TiN (~ 19 W/m-K) by up to a factor of 10. Transmission Electron Microscopy (TEM) was used to characterize film morphology, pointing to additional sources of carrier scattering that might lead to this reduction in conductivity, and suggesting avenues for optimization of growth parameters. The low thermal conductivity of the superlattice films opens up the possibility of using them as bottom electrodes in PCM, towards the goal of reducing power consumption and improving device packing density. A simplified 1D thermal model predicts that reductions in programming current by ~75% are possible.

KEY WORDS: Phase Change Memory, superlattice, thermal conductivity, time-domain thermoreflectance (TDTR)

NOMENCLATURE

C	volumetric specific heat (MJ $m^{-3}K^{-1}$)
I	current (A)
L	thermal penetration depth (m)
R	resistance (thermal: m^2KW^{-1}, electrical: Ω)
d	thickness (nm)
f	frequency (MHz)
k	thermal conductivity ($Wm^{-1}K^{-1}$)

Greek symbols

α	thermal diffusivity (m^2s^{-1})
Φ	diameter of heater element (nm)
ρ	electrical resistivity (μΩ-m)

Subscripts

h	heater
m	melting (current)
p	penetration (depth)
mod	modulation (frequency)
on	electrical resistance in high-field SET state
th,h	thermal resistance of heater
th,GST	thermal resistance of GST

INTRODUCTION

Phase Change Memory (PCM) is a technology that is capable of meeting the scaling needs of the future, with the potential to become a universal Non-Volatile Memory technology [1]. It is based on a change in the electrical resistance of a material due to a temperature induced phase transformation. Chalcogenide materials, which are common PCM active materials, are chemical compounds of group 6B elements with group 3B, 4B, or 5B elements of the periodic table. Although memory switching was observed in these materials as early as the 1960s, it was the recent discovery of fast switching materials such as GST ($Ge_2Sb_2Te_5$) that led to a renewed interest in the commercialization of PCM memory devices [2]. The programming of these devices involves changing the state of the GST material from amorphous to crystalline (SET: high to low resistance state) by heating above the recrystallization temperature and cooling slowly, and from crystalline back to amorphous (RESET: low to high resistance state) by heating above the melting point and cooling rapidly, i.e. quenching. In electrical PCM, this heat is provided externally by means of Joule heating using a current pulse. The amounts of heat injected and contained within the PCM material per unit time are therefore critical parameters that determine how much current is required to affect phase change, i.e. the programming current.

There are three main implications of a lower programming current: 1) a reduction in the energy required to program cells, 2) the elimination of the constraints imposed by the programming current on the scaling of cell selection devices [3] and 3) improvement in device endurance. In the past, several approaches have been demonstrated to reduce programming current [4]. These include reducing the electrode contact area [5][6], scaling the programmed cell volume [7], thermally insulating the electrode [8][9] and engineering the thermal boundary resistance between GST and electrode [10].

In this paper, we explore the possibility of reducing the programming current by designing an electrode that has a reduced thermal conductivity, in this case by replacing the single material electrode TiN, with a multilayer stack of TiN and TaN. A lower electrode thermal conductivity reduces programming current substantially since it increases the thermal resistance and reduces the heat loss through the electrode. Recent research has shown that multilayer stacks of materials offer larger thermal resistance compared to single layer structures, due to additional contribution from the scattering of carriers at interfaces [11]. Moreover, multilayer structures offer the flexibility to choose the top layer to maximize the thermal boundary resistance (TBR) between GST and electrode.

SAMPLE DESIGN

Multilayer samples of TiN/TaN were grown on phosphorous doped silicon wafers by physical vapor deposition. TiN and TaN layers were deposited alternately by DC sputtering of Ti and Ta metals respectively, in N_2 and Ar ambient. Flow rates of 34 and 15 sccm were used for N_2 and Ar respectively; TaN was the topmost layer for all samples (Figure 1).

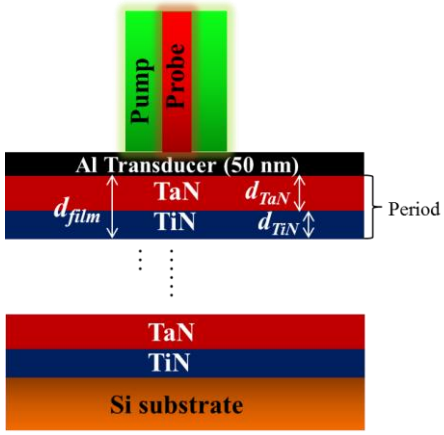

Fig 1 Schematic of samples in cross-sectional view

Other details of growth conditions are provided in Table 1. Also listed are average individual layer, and total film thicknesses as measured from TEM images (Figure 4).

Table 1. PVD growth conditions, and average layer and film thicknesses measured by TEM

#	Power (W) (TiN/TaN)	Dep.Time (s) (TiN/TaN)	d_{TiN}, d_{TiN} (nm)	d_{film} (nm)
1	300/200	40/20	5, 5	365
2	150/150	120/120	7, 25	185
3	150/150	60/120	4, 25	158

In-plane electrical characterization

Sheet resistance measurements were performed on the freshly deposited films using a conventional four-point probe system. Sheet resistance data and the extracted DC in-plane electrical resistivity of the films are given in Table 2. In comparison, the electrical resistivity of TiN typically used as bottom electrode in PCM cells is of the order of ~ 1 μΩ-m [12][13], suggesting that these multilayered TiN/TaN structures have reasonably good electrical conduction properties, at least in the in-plane direction.

Table 2. In-plane electrical resistivity data taken using a four-probe method on freshly deposited films

#	Sheet resistance (Ω/□)	In-plane electrical resistivity (μΩ-m)
1	41.7	15.2
2	45.7	8.5
3	41.0	6.5

TIME DOMAIN THERMOREFLECTANCE

The thermal conductivity of the films in the through-plane direction was measured using time-domain thermoreflectance (TDTR), which is a well-established optical pump-probe technique. Our setup consists of a mode-locked laser emitting 1064 nm pulses at a repetition rate of 82 MHz, with a pulse width of ~ 9 ps. The amplitude of the pump pulses is modulated using an electro-optic modulator at a frequency f_{mod}. This modulation enables high signal-to-noise ratio measurements, and acts as a knob to tune measurement sensitivity to thermal properties at different depths. This is based on the fact that the thermal depth of penetration is $L_p \sim \sqrt{k/\pi C f_{\mathrm{mod}}}$ where k and C are the thermal conductivity and volumetric specific heat respectively. After conversion to 532 nm using a second harmonic generator, the pump pulses are used to heat the sample surface through opto-thermal energy conversion in a ~ 50 nm aluminum transducer. The probe pulses, at 1064 nm measure the transient change in aluminum reflectivity as a function of time delay between the pump and probe pulses, which is varied between 0 to 3.6 ns using a mechanical delay stage. The amplitude of the reflectance oscillations at the f_{mod} harmonic are measured using an RF lock-in amplifier. The data, which consists of the amplitude R as a function of probe delay time, is fit to a multilayer thermal diffusion model that accounts for radial heat conduction, Gaussian laser intensity profiles of pump and probe, and finite thermal interface conductance between different layers, in order to extract one or more unknown thermal properties [14]. These unknown properties may include the conductivity, specific heat of one of the layers, and/or the thermal boundary resistance (TBR) between two layers.

The measurements reported here were made at an f_{mod} of 4 MHz, and using pump and probe laser spot sizes of 10 and 6 μm respectively.

Metrology – Sensitivity Analysis

The sensitivity of the TDTR measurement to a particular thermal property within the stack β may be quantified using the sensitivity coefficient S_β, defined as follows:

$$S_\beta = \frac{\partial \log(R)}{\partial \log(\beta)}, \qquad (1)$$

where R refers to the amplitude signal. Figure 2 shows a plot of S_β as a function of probe delay time. The sensitivity coefficients are plotted for three parameters of interest: the (superlattice) film conductivity k_{film}, the TBR at the aluminum-film interface $TBR_{Al\text{-}film}$, and the TBR at the film-substrate interface $TBR_{film\text{-}Si}$. For the purposes of this sensitivity analysis, the conductivity of the 200 nm thick superlattice film is taken to be 2 W/m-K, with a specific heat of 3 MJ/m^3-K. The baseline values of TBR at the Al-film and film-substrate interfaces are assumed to be 5 m^{2}K/G-W, and f_{mod} = 4 MHz. As seen from the plot, the measurement is fairly sensitive to the film conductivity and the TBR of Al-film, while it is nearly insensitive to the TBR of the film-substrate interface.

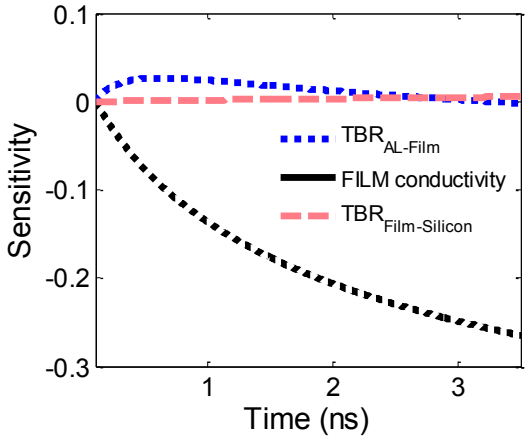

Fig 2 Plot of sensitivity coefficients for k_{film} , $TBR_{Al\text{-}film}$ and $TBR_{film\text{-}Si}$ showing that the measurement is sensitive to the superlattice film conductivity and TBR at the Al-film interface, and insensitive to the TBR at the film-silicon interface.

The analysis of TDTR measurements involves fitting simultaneously for two parameters, k_{film} and $TBR_{Al\text{-}film}$ using a least squares algorithm. The specific heat of the superlattice is taken to be a thickness weighted average of bulk TiN and TaN. Individual layer and film thicknesses are taken from cross sectional TEM images. Table 3 lists these quantities, along with the extracted values of k_{film} and $TBR_{Al\text{-}film}$. Figure 3 shows a representative best fit result for Sample #3. The measured values of k_{film} and $TBR_{Al\text{-}film}$ have error bars of ~ 7 % and 4 % respectively, due to an uncertainty in the thickness of the aluminum transducer (±2 nm).

Table 3. Assumed specific heat C_{film}, and experimental best fit values of the film conductivity k_{film} and thermal boundary resistance between Al and film $TBR_{Al\text{-}film}$ determined from TDTR measurements

#	C_{film} (MJ m^{-3}K^{-1})	K_{film} (Wm^{-1}K^{-1})	$TBR_{Al\text{-}film}$ (m^{2}K GW^{-1})
1	3.06	2.01	5.40
2	2.94	1.57	6.84
3	2.91	1.55	6.98

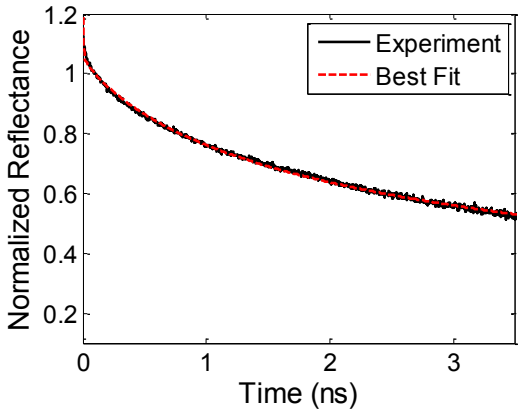

Fig 3 Best fit result for TDTR data taken on Sample #3

We find that the through-plane thermal conductivity of the superlattices lies between 1.5 – 2 W/m-K for the three samples, a reduction by nearly a factor of 10 from the bulk conductivity of TiN (k_{TiN} ~ 19 W/m-K), which is the material commonly used to make bottom electrodes in PCM devices. These values are also slightly reduced from the previously measured values for the intrinsic conductivity of TaN thin films (50 – 100 nm thick) k_{TaN} ~ 3 – 3.5 W/m-K [15].

The thermal conductivity of multilayer films is influenced substantially by the scattering of energy carriers at layer boundaries. The additional resistance offered by boundary scattering decreases the through-plane conductivity from that of the individual bulk materials. This effect is further pronounced when the layer thicknesses are comparable to the dominant carrier mean free path. In material systems where phonons are the predominant heat carriers, previous reports have shown a large reduction in the through-plane conductivity from the thickness weighted bulk averaged value, in some cases by up to an order of magnitude [16][17]. The present material system, i.e. TiN/TaN is more complex due to the fact that both electrons and phonons are expected to contribute to heat conduction within each material. Very little previous work exists on the thermal properties of superlattices of materials that have comparable fractions of heat conducted by both types of energy carriers. A recent study on a Mo/Si multilayer system [18] showed that phonons may contribute to a significant portion of heat conduction within ultra-thin layers of molybdenum, while electrons conduct heat in bulk Mo. Studies such as these suggest that a rich interaction of carriers might be at play in multilayered TiN/TaN films.

In order to provide more insights into the morphological structure of these films, and to obtain an accurate estimate of individual layer and overall film thicknesses, cross sectional transmission electron microscopy (TEM) was performed.

FILM MORPHOLOGY

Figure 4 shows cross sectional TEM images for the three samples, taken at low and high magnification. Besides providing an accurate measure of the thicknesses of individual layers of TiN and TaN and total film thicknesses, the images are informative from the point of view of layer morphology. Images taken at high magnification for all samples show

significant amounts of interface mixing, a feature which may lead to an enhancement in the TiN/TaN thermal boundary resistance. Further, a polycrystalline grain structure is seen within TaN layers, with columnar grains pointed in a direction normal to the growth surface. Apart from grain boundaries and interface mixing, figure 4(b) for the thickest sample (containing 30 periods; period thickness ~ 10 nm) shows a considerable degradation in the film quality beyond the first 5-10 periods. Undulations in the layered structure are amplified with each deposited layer, to the extent that layer continuity is disrupted in several parts of the film. This is an important factor that would need to be considered if such multilayered TiN/TaN films are to be used as electrodes in PCM devices, where electrode thicknesses could be of the order of 200 nm or larger. Slower deposition rates and lower DC power are expected to lead to lesser interface mixing and alloying, hence better quality.

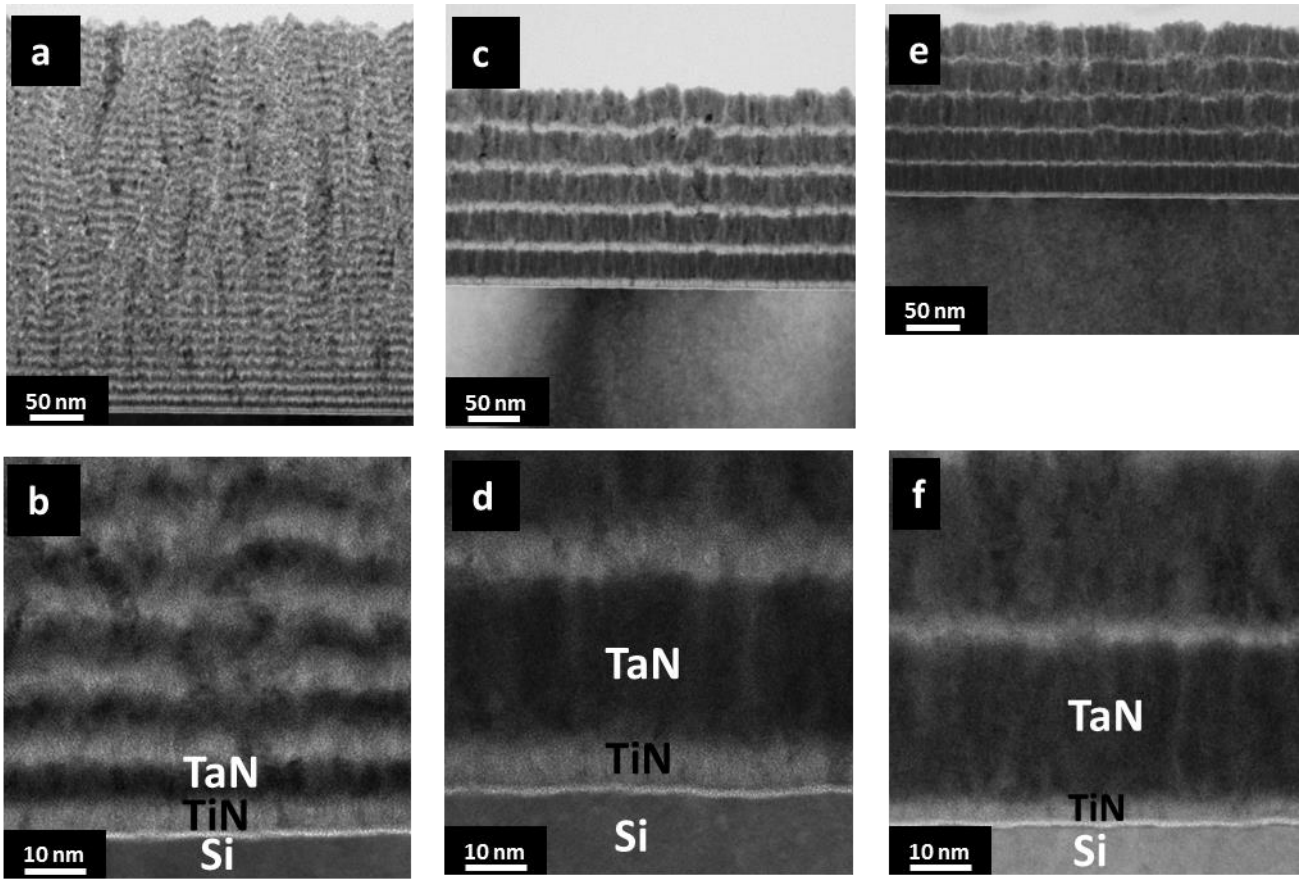

Fig 4 Cross sectional TEM images for (a, b) Sample 1, (c, d) Sample 2, and (e, f) Sample 3. The images in the bottom row are taken at a higher magnification.

IMPLICATIONS FOR PCM DEVICE DESIGN

In order to understand the impact of a lower electrode thermal conductivity on the current required for RESET programming of PCM devices, we invoke a simplified 1D model proposed by Russo et al. [19]. The main assumptions made in this model are that 1) RESET current is the current required to melt PCM (I_m) [19], 2) the entire heat generated within the heater is delivered to the GST-heater interface, which is at the peak GST melting temperature (888 K), and that 3) the lateral temperature gradients within the heater are negligible. Under these conditions, I_m can be calculated in terms of the effective parallel thermal resistance through the heater and GST, and the high-field electrical resistance of the cell R_{on}. Figure 5 shows a schematic of this model along with the equivalent thermal circuit model. In this model, we assume a lance-type PCM cell, with dimensions as shown in Figure 5. The thermal conductivity of the GST in the SET state is taken to be 1 W/m-K. The melting current I_m is calculated for a range of heater thermal conductivities, at a fixed device electrical resistance. Since the device electrical resistance in the SET state is dominated by the resistance of the heater, this can be calculated directly based on the heater resistivity and aspect ratio. In Figure 6, we plot I_m versus heater thermal conductivity k_h for two different heater resistivities ρ_h = 1 μΩ-m and 10 μΩ-m. The former corresponds to the typical electrical resistivity of bulk TiN, while the latter corresponds to the average value measured for our TiN/TaN superlattice

films. Points marked by the blue and red squares represent the cases for bulk TiN and nanostructured TiN/TaN electrode respectively, showing an expected reduction of about 75 %.

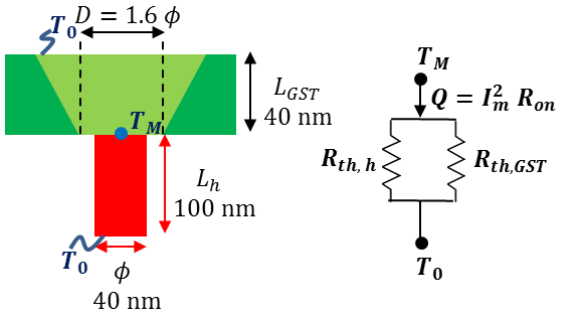

Fig 5 Simplified thermal model (see [19])

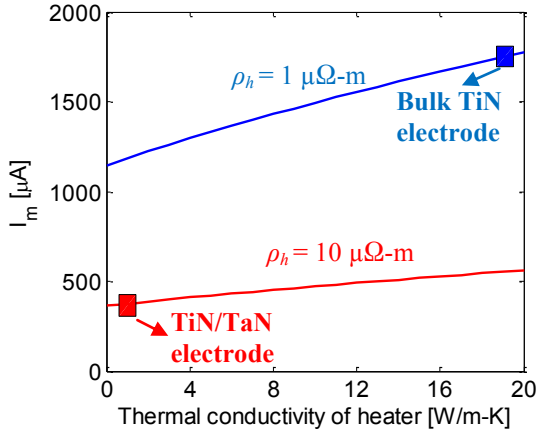

Fig 6 Melting (RESET) current predicted by the simplified thermal model for two cases of heater resistivity (blue: ρ_h = 1 μΩ-m and red: ρ_h = 10 μΩ-m). The blue and red squares represent the cases corresponding to bulk TiN (k_h ~ 19 W/m-K) and superlattice TiN/TaN electrodes (k_h ~ 1 W/m-K), respectively.

CONCLUSIONS

In this paper, we have investigated the feasibility of using multilayered films of TiN/TaN as bottom electrical contacts in PCM devices. We have shown that such multilayered structures, with period thicknesses down to 10 nm have a through-plane thermal conductivity that is reduced by up to an order of magnitude from bulk TiN. A previous study that used a ~5 nm TaN insulting layer encapsulating a ~4.5 nm thick TiN ring electrode achieved a 10 fold reduction in the reset current over a solid TiN bottom electrode [8]. We expect that using a multilayered TiN/TaN electrode design would further reduce operating current. This would lead not only to an improvement in the device efficiency, but also an enhancement in the cycling endurance, since lower currents lead to lesser electromigration damage. A simplified 1D thermal model predicts a scaling of the programming (RESET) current with heater conductivity, suggesting that a reduction of ~75 % is achievable.

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