

IN-PLANE THERMAL CONDUCTIVITY MEASUREMENT ON NANOSCALE CONDUCTIVE MATERIALS WITH ON-SUBSTRATE DEVICE CONFIGURATION

Takashi Kodama, Woosung Park, Amy Marconnet, Jaehoo Lee, Mehdi Asheghi, Kenneth E. Goodson
Department of Mechanical Engineering, Stanford University
440 Escondido Mall
Stanford, CA 94305, USA
Phone: (650) 736-1283
Fax: (650) 723-7657
Email: kodama@stanford.edu

ABSTRACT

In this study, we measure the in-plane thermal conductivity of palladium (Pd) nanowire with varying length (3-50 μm) and width (100-250 nm). The bridges are fabricated by electron beam lithography with an on-substrate measurement configuration. The measurements are performed on substrates with 190 nm and 2.9 μm thick thermal oxide using a 4-probe steady-state DC Joule heating method, and several suspended structure are also prepared to investigate the accuracy of the on-substrate results. For the on-substrate measurements, the thermal conductivity is estimated for short nanowires assuming the magnitude of the heat loss to the substrate from measurements of longer nanowires. As a result, the measured thermal conductivity is 30 ± 5 W/mK for suspended short nanowires at room temperature, and the estimated thermal conductivity for the on-substrate samples are consistent with this value. The measurements on the substrate with 2.9 μm oxide result in small variations between samples (± 5 W/mK), while the results on 190 nm thick oxide has a larger variation and uncertainty ($> \pm 20$ W/mK) due to the uncertainty in the magnitude of the heat loss to the substrate. Sufficient measurement accuracy is only achieved if the heat loss to the substrate can be estimated or measured with high accuracy.

KEY WORDS: Nanowire, in-plane thermal conductivity, Joule heating measurement, electron beam lithography, nanofabrication, nanolithography

NOMENCLATURE

A	cross sectional area, m^2
w	width, m
L	length, m
d	thickness, m
k	thermal conductivity, W/mK
g	Heat loss per unit length W/mK
p	Heat generation per unit length, W/mK
R	electrical resistance, Ω
T	temperature, K
I	current amplitude, A
V	bias voltage, V
x	position, m
m	temporal variable

Greek symbols

α	temperature coefficient of resistance, $/\text{K}$
ϕ	shape factor

ρ	thermal resistivity, $\text{m}^2\text{K/W}$
σ	electrical conductivity, S/m
θ	temporal variable
a	ambient
s	sample

Subscripts

oxide	thermal oxide
0	bulk temperature
TB	thermal boundary resistance
si	silicon substrate
sub	substrate
TB	thermal boundary resistance
2D	2 dimensional heat spreading effect

INTRODUCTION

Recent improvements in nanofabrication and chemical synthesis technology enable fabrication of a wide variety of nanomaterials such as nanowires and ultra thin films. Their unique physical properties, which differ from those of bulk materials, make nanomaterials attractive for various industrial applications. In addition to their versatile electrical properties, thermal conduction in nanomaterials has been of considerable interest. Carbon nanotubes [1-3] and graphene [4,5] have extremely high thermal conductivities, while silicon nanostructures are being considered as inexpensive thermoelectronics materials since the thermal conductivity can be considerably depressed due to size effects (phonon scattering), while the electrical conductivity remains high [6-8]. Despite the potential capabilities of other nanomaterials, their thermal conductivities have not yet been reported due to challenges in fabricating thermal conduction measurement structures.

For thin films, measurement techniques based on controlling the heat penetration depth, such as thermoreflectance [9] and 3ω method [10], are effective for determining the out-of-plane thermal conductivity [11]. It is also possible to measure the in-plane thermal conductivity by reducing the size of the heating spot [12], if the required size is larger than the diffraction or fabrication limit. However, it is difficult to apply these traditional thin film measurement technique to isolated nanomaterials. Additionally, in order to measure the in-plane thermal conductivity, the samples generally have to be suspended to eliminate the heat conduction path to the substrate [13,14]. However, the

suspended bridge structure is often hard to fabricate because the nanowires often break due to mechanical stress or the damage to the nanowire from the chemicals used to suspend it.

Therefore, in this study, we measure the in-plane thermal conductivity with an on-substrate configuration for palladium (Pd) nanowires fabricated by electron beam (e-beam) lithography. The measurement accuracy is investigated by accounting for the heat loss through the substrate.

EXPERIMENTAL

- Device Fabrication:

All Pd nanowire devices are fabricated by the combination of photolithography and e-beam lithography. First, a thermal oxide layer (190 nm or 2.9 μm thick) is grown on standard silicon wafers by wet oxidization. Large metal (25 nm Pt with 5 nm Cr adhesion layer) lines, for electrical probe connections, are patterned on both substrates by photolithography. Finally, the nanoscale Pd structures, including the nanowire and connections from the nanowire to the Cr/Pt probe connections) are fabricated by e-beam lithography. Both sets of metal lines are fabricated with a lift-off process. The thickness of Pd nanowires, d , is 40 nm for all devices, and the length, L , and width, w , are varied from 3 to 50 μm and 100 to 250 nm, respectively. Their width and thickness are measured after fabrication by using scanning electron microscopy (SEM) and atomic force microscopy, respectively, and the measured values are used for the thermal analysis.

To investigate the accuracy of on-substrate measurements, several suspended structures are also fabricated. The entire Pd nanowire device is covered with an e-beam resist and only the resist surrounding the nanowires is exposed with e-beam lithography. The thermal oxide and bottom silicon substrate in this exposed region are etched using buffered oxide etchant (an isotropic etchant) and then XeF_2 gas. Finally, the remaining e-beam resist is removed from the surface with an acetone.

- Measurement Procedure:

The thermal conductivity of nanowires were measured by 4-probe Steady-state DC Joule heating technique [14,15]. All measurements were performed under ambient environment at room temperature (295 K), and convective and radiative heat losses are neglected. The temperature coefficient of electrical resistance (TCR) is measured on 7 randomly selected devices within the temperature range of 295-320 K. The average TCR is $0.00175 \pm 0.0002 \text{ K}^{-1}$, with no length or width dependence, and is used for all analysis.

RESULTS AND DISCUSSIONS

A schematic of the Pd nanowire device layout and topographic images, taken by scanning electron microscopy, are shown in Fig. 1. The lengths of prepared nanowires are 3, 4, 6, 10, 20, 30, 40, and 50 μm . The narrow voltage pads are connected to the end of the nanowires, and the current pads are > 10 times wider than the nanowire width, w , in order to minimize heat generation in these probe connections. Same structures are prepared on both 190 nm and 2.9 μm thick SiO_2 with several nanowire widths ($w = 100, 150, 200$, and 250 nm),

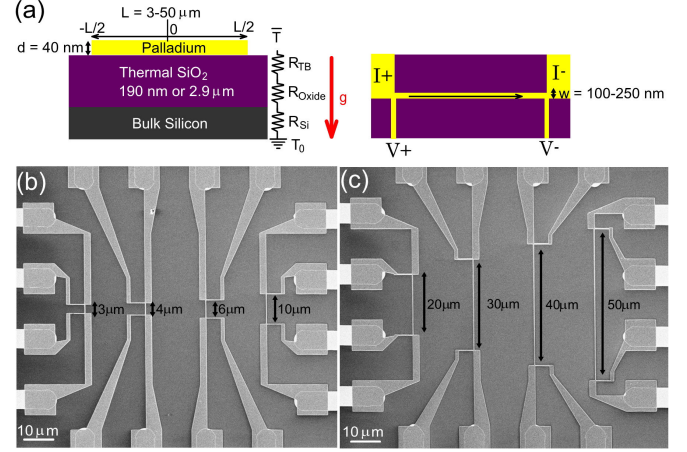


Fig. 1 (a) A schematic of the device structure and measurement. (b), (c) Representative SEM images of Pd nanowire devices fabricated on 190 nm thick SiO_2 . The width and thickness of Pd nanowires are 100 and 40 nm, respectively, and the length is 3, 4, 6, 10, 20, 30, 40 and 50 μm from left side.

and I-V curve are measured for the estimation of the thermal conductivity.

The heat conduction along the Pd nanowires in the on-substrate configuration is expressed by the following steady state one-dimensional heat diffusion equation with the boundary condition of $T(x = \pm L/2) = T_0$ [2].

$$k_s A \frac{d^2 T(x)}{dx^2} + p'[1 + \alpha(T(x) - T_0)] - g(T(x) - T_0) = 0 \quad (1)$$

where k_s , $A = wd$, and α are the thermal conductivity, cross-sectional area and TCR of the sample, respectively, g is the heat loss per unit length to the substrate, $T(x)$ is the temperature profile along the length of the nanowire, $T_0 (= 295 \text{ K})$ is the substrate temperature, and $p' = I^2 R_0 / L$ is the heat generation per unit length in the sample where I and R_0 are current amplitude and the electrical resistance of the sample at T_0 , respectively.

Assuming $\theta(x) = p'[1 + \alpha(T(x) - T_0)] - g(T(x) - T_0)$, then equation (1) reduces to

$$\frac{d^2 \theta(x)}{dx^2} = \frac{1}{m^2} \theta(x) \quad (2)$$

where $m^2 = (g - \alpha p') / k_s A$ when $g - \alpha p' > 0$. The general solution of equation (2) is

$$\theta(x) = p' \frac{\cosh(mx)}{\cosh(mL/2)}$$

or

$$T(x) = T_0 - \frac{p'}{g - \alpha p'} \left(\frac{\cosh(mx)}{\cosh(mL/2)} - 1 \right) \quad (3)$$

Integrating the equation (3) from $x = -L/2$ to $L/2$, the average temperature along the nanowires is given by

$$\bar{T} = T_0 - \frac{p'}{g - \alpha p'} [(2/mL) \tanh(mL/2) - 1] \quad (4)$$

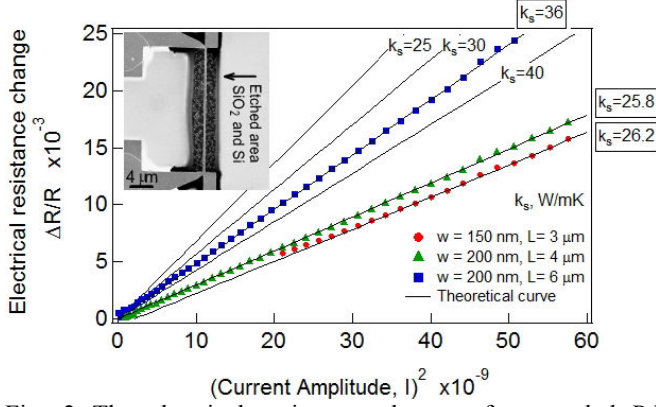


Fig. 2 The electrical resistance change of suspended Pd nanowires by Joule heating. The vertical and lateral axis corresponds to the ratio of the relative electrical resistance change $\Delta R (= R - R_0)$ to R and square of the current amplitude, respectively. The red circles, green triangles, and blue squares correspond to the experimental data taken on the devices, and their length and width of nanowires are shown in the figure. Solid black line is the theoretical curve obtained by the formula (6). The representative SEM image of the suspended Pd nanowires is shown.

Combining the temperature profile with $\bar{R} = R_0 [1 + \alpha(\bar{T} - T_0)]$, the average electrical resistance under during Joule heating is given by

$$\bar{R} = R_0 \left(1 + \frac{\alpha p'}{g - \alpha p'} \right) - R_0 \cdot \frac{\alpha p'}{g - \alpha p'} \left[(2/mL) \tanh(mL/2) \right] \quad (5)$$

In order to investigate the accuracy of the present on-substrate measurement method, the thermal conductivity of suspended Pd nanowires are also measured. The heat conduction along the suspended nanowires is also expressed by equation (1) with no heat loss to the substrate ($g=0$). In this case, the average electrical resistance is given by [14,15]

$$\bar{R} = R_0 \cdot \left[(2/mL) \tanh(mL/2) \right] \quad (6)$$

where $m^2 = \alpha p' / k_s A$.

Figure 2 shows the relative change in electrical resistance due to Joule heating for suspended Pd nanowires as a function of a square of current amplitude. By fitting (6) to the experimental data, the thermal conductivity of suspended samples with length, $L = 3, 4$, and $6 \mu\text{m}$, are estimated to be 26.2, 25.6 and 35.8 W/m/K, respectively. The analytical error from the data fitting is below 0.1 %. The 1% uncertainty in TCR yields an additional uncertainty in the measured thermal conductivity (± 4 W/m/K). There is no length or width dependence on the electrical conductivity, σ_s . As shown in Figure 3, the average electrical conductivity is $4.7 \times 10^6 \pm 0.6 \times 10^6$ S/m. From this measured electrical conductivity, the predicted thermal conductivity at 295 K is 34 ± 4.5 W/m/K according to the Wiedemann-Franz Law given the Lorenz number of $2.44 \times 10^{-8} \text{ W}\Omega/\text{K}^2$ [16]. Thus, there is an intrinsic variation in k_s between each device. Therefore, the estimated values for the k_s for the suspended nanowires are considered to be within the limit of the error for all three lengths. For bulk Pd, the reported electrical and thermal conductivity of are 9.5

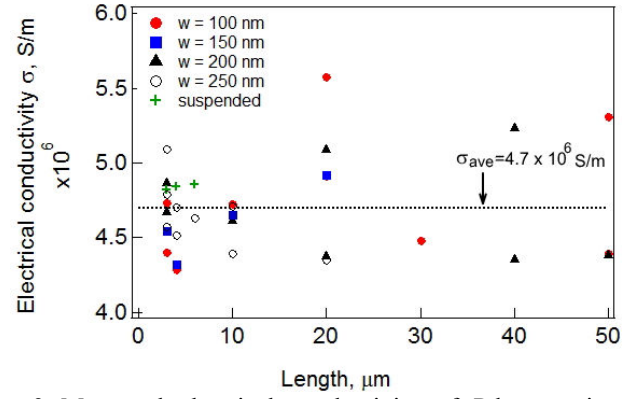


Fig. 3 Measured electrical conductivity of Pd nanowires. Experimental data measured on suspended device, on both 2.9 μm and 190 nm thick oxide are shown in the graph.

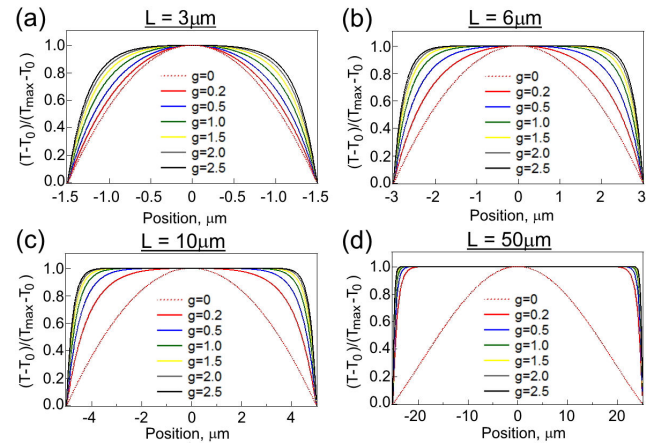


Fig. 4 Theoretical temperature distribution on the Pd nanowires with the variation of the heat loss to the substrate g . (a), (b), (c) and (d) are temperature profile when the length L is 3, 6, 10, 50 μm , respectively. These were created by the formula (3) when $A = 4 \times 10^{-15} \text{ m}^2$, $I = 100 \mu\text{A}$, $\alpha = 0.00176 \text{ K}^{-1}$, $k_s = 35 \text{ W m}^{-1} \text{ K}^{-1}$, and $\sigma_s = 4.7 \times 10^6 \text{ S m}^{-1}$. The vertical axis corresponds to the ratio of the temperature variation $(T - T_0)$ to the maximum value $(T_{\max} - T_0)$ on the nanowires.

$\times 10^6$ S/m and 71.8 W/m/K, respectively [16], twice as large as measured for the nanowires. Previous studies of thin Pd films have shown that the electron mean free path is about 10 nm in bulk Pd and that the thin film electrical conductivity considerably decreases when the thickness ~ 10 nm [17]. Since the thickness and width of Pd nanowires in this work are sufficiently larger than 10 nm, the reduction of the conductivity likely does not originate from the size effect but from the deterioration of the film quality in these narrow structures fabricated by the lift-off method.

Figure 4 shows the theoretical temperature profile along the nanowire on substrates caused by the self Joule heating as a function of heat loss to the substrate and nanowire length. The temperature profile is flat at the center of the sample, and the proportion of the nanowire with a small thermal gradient increases as g and L increase. In this region of the temperature profile, the heat generation in the nanowire is proportional to the heat loss to the substrate because there is no temperature

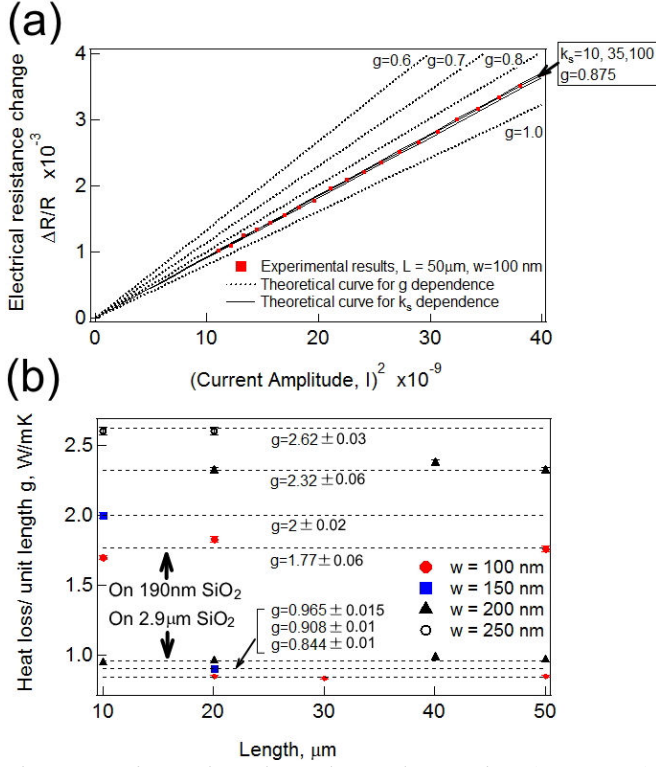


Fig. 5 Experimental results on long Pd nanowires ($L \geq 20 \mu\text{m}$). (a) Representative DC Joule heating measurement results of Pd nanowires on substrate (on $2.9 \mu\text{m}$ oxide) and curve fit by the equation (5). (b) Length dependence of an heat loss per unit length to the substrate, g , obtained from the experimental data on long Pd nanowires.

variation at in-plane direction. Assuming $k_s A d^2 T(x)/dx^2 \approx 0$, the heat diffusion equation in Eq. (1) becomes approximately.

$$p'[1 + \alpha(T(x) - T_0)] \approx g(T(x) - T_0) \quad (7)$$

Since the temperature profile is mostly flat along the nanowire the majority of the nanowire for long lengths ($L > 20 \mu\text{m}$, see Fig. 2c and 2d), the overall thermal conduction in these nanowires is dominated by the heat loss to the substrate. On the other hand, contribution of in-plane thermal conduction is significant in shorter nanowires. Thus, the following method is taken in order to estimate k_s with on-substrate configuration.

- (i) Assuming uniform k_s , p' , and g along the nanowire, the heat loss to the substrate is estimated by fitting Eq. (6) to the experimental data for long nanowires (assuming an arbitrary value of k_s).
- (ii) By fitting (6) to the data for on shorter samples, k_s is estimated with the obtained g from step (i).
- (iii) Using an iterative process, g and k_s are determined self-consistently for both short and long samples.

Figure 5 shows the experimental results and analytical solutions for long nanowires ($L \geq 20 \mu\text{m}$). As shown in Fig. 5a, the theoretical curve is insensitive to variations of thermal conductivity, but the slope of the theoretical curve is remarkably sensitive to small variations in magnitude of the

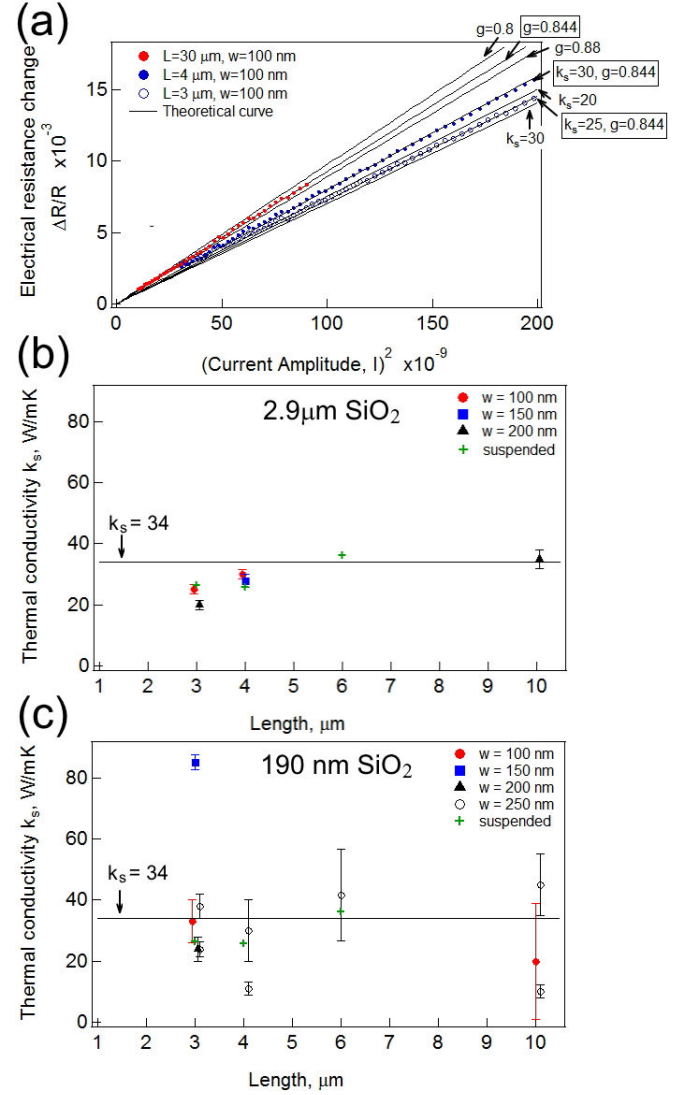


Fig. 6 Experimental results on long Pd nanowires ($L \geq 20 \mu\text{m}$). (a) Representative DC Joule heating measurement results of Pd nanowires on substrate (on $2.9 \mu\text{m}$ oxide) and curve fit by the equation (5). (b) Length dependence of an heat loss per unit length to the substrate, g , obtained from the experimental data on long Pd nanowires.

heat loss to the substrate. This analysis is applied to all data for long nanowires with the assumption of $k_s = 35 \text{ W/mK}$, and the estimated values of g are summarized in Fig. 5b. For each nanowire width, the magnitude of the substrate heat loss is nearly constant for nanowire lengths between 20 and $50 \mu\text{m}$. Further, due to the difference of the thermal resistance, the estimated g on 190 nm thick SiO_2 is larger than for the $2.9 \mu\text{m}$ thick SiO_2 . The average values of g for each nanowire width and oxide thickness are summarized in Figure 5b. The error bars include uncertainty both from the data fitting and from the small variations between the data points at different nanowire lengths.

Next, in-plane thermal conductivity is estimated from the data measured for shorter nanowires ($L \leq 10 \mu\text{m}$) with the extracted g from the long nanowire measurements. Figure 6a

shows a representative data set for the estimation of thermal conductivity and substrate conductance for a 100 nm wide nanowire on the substrate with 2.9 μm SiO_2 . First, from the data on the long nanowire ($L=30 \mu\text{m}$), the g is estimated to be $0.844 \pm 0.01 \text{ W/mK}$. From the shorter nanowires ($L = 3$ and $4 \mu\text{m}$), k_s is estimated to be $25 \pm 1.0 \text{ W/mK}$ and $30 \pm 1.5 \text{ W/mK}$, respectively. These values are consistent with the value of k_s used to estimate g from the long nanowire data. This analysis was applied to all data sets, and the estimated thermal conductivities are summarized in Figs. 6b and 6c. Fig. 6b shows that the estimated k_s on 2.9 μm SiO_2 are consistent with the values measured for suspended nanowires with small variations in the range of the measurement uncertainty discussed above. The analytical error is $<1\%$ when sample length is in the range of 3–6 μm , and there is no remarkable width and length dependence on the results. On the other hand, for the measurements with 190 nm SiO_2 , the variation and uncertainty in k_s is larger than for 2.9 μm SiO_2 (see Fig. 6c). The uncertainty in g impacts the accuracy in k_s , and a large conductance to the substrate leads to larger uncertainty in k_s . For example, when $w=100 \text{ nm}$ and $L=3 \mu\text{m}$, the estimated g for 190 nm and 2.9 μm SiO_2 were 0.844 and 1.77 W/mK , respectively. Assuming 10% uncertainty in g , the resulting uncertainty in k_s would be about 50 and 80% ($k_s = 25 \pm 12$, $32 \pm 25 \text{ W/mK}$), respectively. Further, as shown in Figs. 6b and 6c, the error becomes larger as the sample is longer because of the higher contribution of g . The thermal resistivity of the substrate corresponds to w/g , and for 2.9 μm SiO_2 , since boundary resistance between the oxide and the silicon substrate can be neglected, the total thermal resistivity is expressed by

$$w/g = \rho_{TB} + \rho_{\text{oxide},2D} = \rho_{TB} + \frac{d_{\text{oxide}}}{k_{\text{oxide}} \cdot \phi} \quad (7)$$

where ρ_{TB} and $\rho_{\text{oxide},2D}$ are the thermal boundary resistivity between the Pd nanowire and SiO_2 layer and the thermal resistivity of silicon dioxide including 2D heat spreading effect, respectively, and $d_{\text{oxide}} (= 2.9 \mu\text{m})$, $k_{\text{oxide}} (= 1.4 \text{ W/mK})$, and ϕ are the thickness, bulk thermal conductivity of SiO_2 , and shape factor [18] (determined by w/d_{oxide}), respectively. From equation (8), theoretical $\rho_{\text{oxide},2D}$ is estimated to be 124.7, 176.1, 213.0 $\text{m}^2\text{K/GW}$ when the width of nanowire is 100, 150, and 200 nm, respectively. By substituting these values and the experimentally obtained total heat loss (g) into (8), the ρ_{TB} is calculated to be 50.2 ± 4 , 50.1 ± 6 , $58.7 \pm 10 \text{ m}^2\text{K/GW}$, respectively. There is no width dependence in the boundary resistivity and the value agrees well with typical thermal boundary resistance values [19–21]. In the present measurement, the ρ_{TB} corresponds to over 20% of total thermal resistance. Thus, it is impossible to ignore the value for the estimation of k_s due to the production of large uncertainty. While the $\rho_{\text{oxide},2D}$ could be theoretically predicted with high accuracy, it is difficult to predict the ρ_{TB} with sufficient accuracy because small variations in the device fabrication and materials significantly impact boundary resistance. Therefore, it is necessary to measure the boundary resistance experimentally with the different materials and geometries.

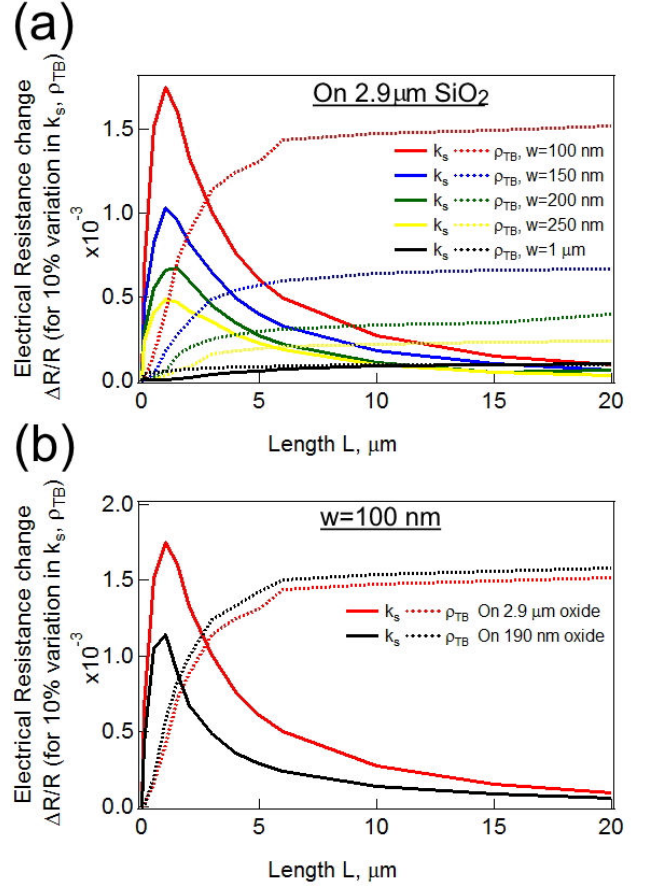


Fig. 7 Measurement sensitivity for the in-plane thermal conductivity measurement with on-substrate device configuration. (a), (b) Theoretical relative electrical resistance change in the Pd nanowires for 10% variation in thermal conductivity, k_s , and thermal boundary resistivity, ρ_{TB} , as function of wire length, L , and width, w . All curves are created by 3D simulation with COMSOL 4.2a. The parameters used in these simulations are: $d_s = 4 \times 10^{-8} \text{ m}$, $I = 100 \mu\text{A}$, $\sigma_s = 4.7 \times 10^6 \text{ S m}^{-1}$, $\alpha = 0.00176 \text{ K}^{-1}$, $k_s = 35 \text{ W m}^{-1} \text{ K}^{-1}$, and $\rho_{TB} = 20 \text{ m}^2 \text{ K (GW)}^{-1}$.

Figure 7 shows the relative electrical resistance change for 10% variation in k_s and ρ_{TB} as a function of a sample length obtained by 3 dimensional finite element models (using COMSOL 4.2a). The relative electrical resistance change corresponds to the measurement sensitivity. As shown in Fig. 7a, the sensitivity in k_s decreases as the length increases and contribution of the boundary resistance increases. As shown in Fig. 7b, the relative sensitivity of k_s to the thermal boundary resistance decreases as the oxide thickness decreases because of the increased contribution of the substrate heat loss. As indicated in Figure 7a, the measurement is more sensitive to the thermal conductivity and heat loss to the substrate for narrower nanowires. In fact, at the limit of structures that can be fabricated by conventional photolithography (1 μm), the electrical resistivity is not sensitive to either property for any length. Therefore, this on-substrate thermal conductivity measurement technique is only applicable for nanoscale samples

In this study, we present the in-plane thermal conductivity measurement of conductive nanomaterials with on-substrate device configuration. Sufficient measurement accuracy is only achieved if the heat loss to the substrate can be estimated or measured with high accuracy. The measurement accuracy will be improved if the ratio of the thermal conductance of the sample to that of the substrate is large. Several parameters of both the sample and measurement device configuration must be controlled to minimize measurement uncertainty. Therefore, the device design must be optimized for each target material in order to obtain sufficient measurement sensitivity.

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