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Thermoelectric Characterization and Power Generation Using a Silicon-on-Insulator Substrate

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***Abstract*—We demonstrate techniques for measuring thermoelectric voltages and generating on-chip power using a silicon-on-insulator substrate. Our design uses lateral heat conduction in the silicon overlayer to establish temperature gradients, which dramatically reduces microfabrication complexity compared to competing designs based on a free-standing membrane. This letter characterizes the thermoelectric power of a metal–semiconductor structure involving a doped SbTe alloy that is relevant for phase-change memory. The thermoelectric power of the SbTe–TiW thermocouple is 24 μV/K, and the power generation output achieves up to 0.56 μW/cm^2 with a temperature gradient of 18°K. [2011-0233]**

***Index Terms*—On-chip power generation, SbTe, Seebeck coefficient measurement, silicon-on-insulator (SOI), thermoelectric power generation (TEG).**

I. Introduction

The demand for thermoelectric materials, which convert heat to electricity, continues to grow. Novel materials are being developed to meet this need, and the dimensionless figure of merit ($ZT = S^2\sigma T/k$) for thin films has improved up to 2.4 [1]. Thermoelectric properties are particularly important for phase-change memory, a potential building block for ultradense data storage. Experimental evidences show that the thermoelectric effects can strongly influence the device performance [2], [3]. However, the literature lacks the thermoelectric properties of thin-film phase-change materials.

While measurement techniques for electrical and thermal conductivities (σ, k) are available in various forms, the thermoelectric power (S) has received relatively little attention. Bulk measurements are not suitable for thin films or nanostructured materials. The conventional approach requires underetching to make a free-standing membrane [6]–[10], and some rely on special instrumentation such as scanning microscopy [4] and phase lock-in circuitry [5]. Here, we demonstrate a technique for measuring the thermoelectric power of thin-film materials using a silicon-on-insulator (SOI) substrate. The SOI substrate provides the necessary temperature gradient by optimizing lateral heat conduction in the silicon overlayer. The SOI-based device can also offer on-chip thermoelectric power generation (TEG) with significantly reduced microfabrication overhead and cost compared to competing designs based on free-standing membranes [10]–[12]. This work characterizes the thermoelectric power and the TEG output of SbTe–TiW thermocouples using the resistance thermometry and the infrared (IR) microscopy.

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II. Experimental Methods

A. Design and Fabrication

Samples are prepared on a SOI substrate with an 8-μm-thick silicon layer and a 3-μm-thick buried oxide layer. The silicon overlayer provides excellent lateral conduction but lowers heat generation in the heater. The thick buried oxide layer ensures modest levels of temperature rise. A 100-nm-thick oxide is deposited on the SOI substrate for electrical passivation. A 50-nm-thick TiW film is then deposited and patterned into electrodes. The TiW serves as heaters, thermometers, and the thermoelectric leg. The other thermoelectric leg is formed by a 20-nm-thick doped SbTe alloy. The number of SbTe–TiW pairs varies from one to seven for measurement validation. Subsequent deposition of 100-nm-thick nitride and 300-nm-thick oxide prevent any surface contamination.

The experimental structure [Fig. 1(a)] optimizes the heat spreading such that the hot junction of the thermocouple experiences a large temperature rise while the cold junction is at the substrate temperature, eliminating the need for a second thermometer. The SOI substrate offers an attractive platform compared to conventional structures [Fig. 1(b)]. For example, heaters on silicon substrates lose the majority of heat within the first few micrometers. Free-standing membranes can provide the largest temperature gradient but are limited by processing techniques, which require the membranes to be suspended up to the cold junction of thermocouples. By controlling the silicon and oxide layer thicknesses, the SOI-based design can achieve the necessary temperature gradient without requiring underetching.

B. Thermal Healing Length Estimations

The temperature rise (θ) of SOI substrate in the lateral direction (x) can be estimated using a thermal healing length (L_h) approximation [13]

$$\theta(x) = \theta_b \exp\left(-\frac{x}{L_h}\right)$$

where

$$L_h \approx \sqrt{\frac{k_{\mathrm{Si}} d_{\mathrm{Si}} d_{\mathrm{SiO_2}}}{k_{\mathrm{SiO_2}}}} \tag{1}$$

where θ_b is the temperature rise in the silicon layer right below the heater and k_{Si}, k_{SiO2}, d_{Si}, and d_{SiO2} are the thermal conductivities and the thicknesses of the silicon overlayer and the buried oxide layer, respectively. The thermal healing length characterizes the length scale of temperature decay. A long thermal healing length ensures large temperature rise at the hot junction. However, the temperature gradient can also decrease when the heat reaches the cold junction. The

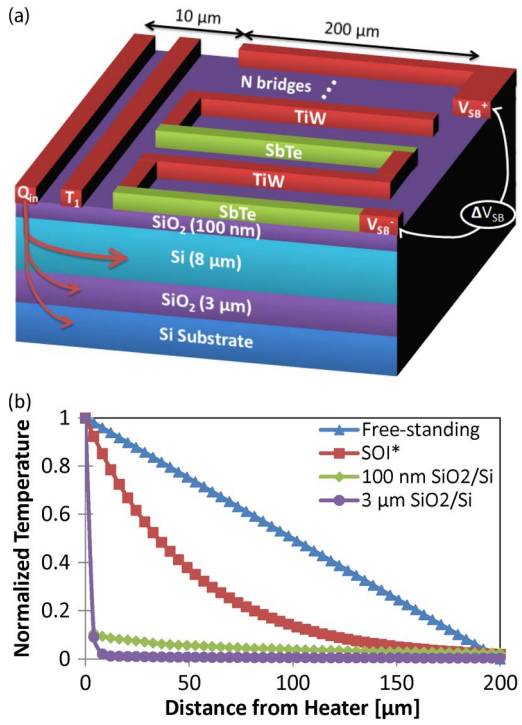

Fig. 1. (a) Schematic of experimental structure for measuring the thermoelectric voltage, with a varying number of SbTe–TiW thermocouples. The figure is not drawn to scale. (b) Predicted temperature profiles for the SOI-based structure and conventional measurement structures. Heat spreading in the SOI substrate is comparable to that of a free-standing membrane and superior to Si substrates.

TABLE I
THERMAL HEALING LENGTH (L_h) OBTAINED BY VARIOUS METHODS

Approximation (in Eq. 1)	Finite Element Simulation	Electrical Resistance Thermometry	Infrared Microscopy
51 μm	64 μm	61 μm	63 μm

approximation in (1) requires a negligible temperature drop across the silicon layer thickness, an infinitely long silicon layer, and all the heat dissipation to the buried oxide layer. This results in a smaller thermal healing length estimate (Table I).

Samples with thermometers patterned at different distances from the heater are used to experimentally determine the thermal healing length. After the temperature coefficient of resistance (TCR) calibration, the temperature rise is measured with increasing heating power (Fig. 2). The exponential fit to these data yields a thermal healing length of 61 ± 8 μm. The finite-element simulation results match closely with the electrical resistance thermometry data using the nominal thermal conductivity values 149 and 1.4 W/mK for silicon and for SiO_2, respectively, at room temperature. The thermal healing length allows a significant temperature rise at the hot junction, while the cold junction temperature is less than 4.8% of the total temperature.

C. In Situ IR Microscopy

In situ IR microscopy verifies the temperature distribution throughout the device during the thermoelectric voltage measurement. The IR microscope has a temperature sensitivity of 0.1 K and a spatial resolution of about 2 μm. The resolution should be much smaller than the thermal healing length to resolve the temperature distribution. Prior to measuring the operating device, the surface emissivity is calibrated

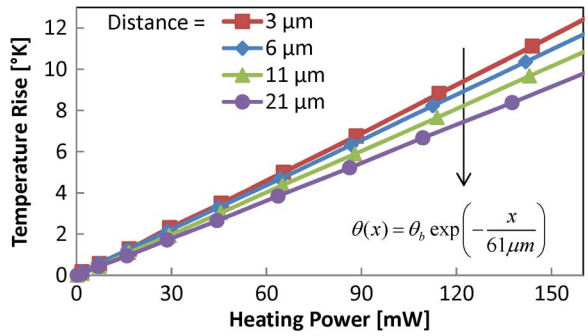

Fig. 2. Estimation of the healing length using the temperature rise as a function of heating power at several distances from the heater. The exponential fit to these data estimates that the thermal healing length is 61 μm.

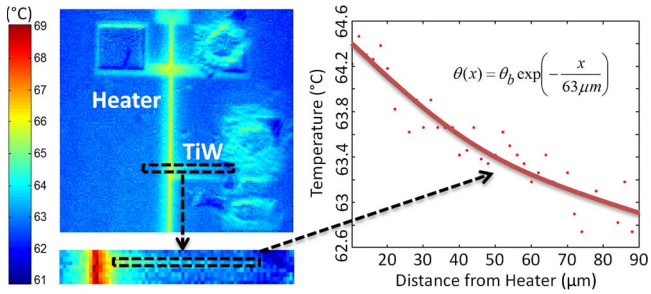

Fig. 3. IR imaging of the thermoeletric voltage measurement. The temperature gradient along the thermocouple is shown in the plot to the right, and the thermal healing length is approximately 63 μm.

by heating the sample to a uniform temperature and recording a reference image. A surface emissivity map then relates the radiance of each point to the temperature. Fig. 3 shows the temperature along the TiW electrode and a least squares fit to the exponential decay. The thermal healing length estimated from this fit is 63 μm, which corresponds well with the electrical resistance thermometry and the simulation results.

III. THERMOELECTRIC CHARACTERIZATION

The heat spreading from the resistive heater produces a temperature gradient and the thermoelectric voltage across thermocouples. A combination of (1) and the temperature measurement at 3 μm from the heater provides the hot junction temperature. Fig. 4 shows that the thermoelectric voltage increases proportionally with the temperature rise and the number of SbTe–TiW pairs by 24.0 ± 1.5 μV/K per pair. To extract the Seebeck coefficient of individual materials, another combination of materials, where one of them is a reference material with known Seebeck coefficient, should be tested.

The major source of uncertainties stems from the temperature calibration of resistive thermometers. The measured TCR of each thermometer is accurate to 2% uncertainty. An uncertainty of up to 28% for the thermal healing length results from the exponential fit using the four thermometers at varying distance from the heater. The thermal healing length uncertainty translates into the uncertainty of 5% for the hot junction temperature. Combined with other sources of uncertainties, such as voltage fluctuations and processing variations, the total uncertainty of the thermoelectric power measurement is 12.5%.

TEG is measured on an external load with varying resistance [Fig. 4(b)]. Impedance matching with the internal resistance (6 kΩ) produces the maximum output power. A single SbTe–TiW thermocouple achieves up to 0.56 μW/cm^2 power output with a temperature

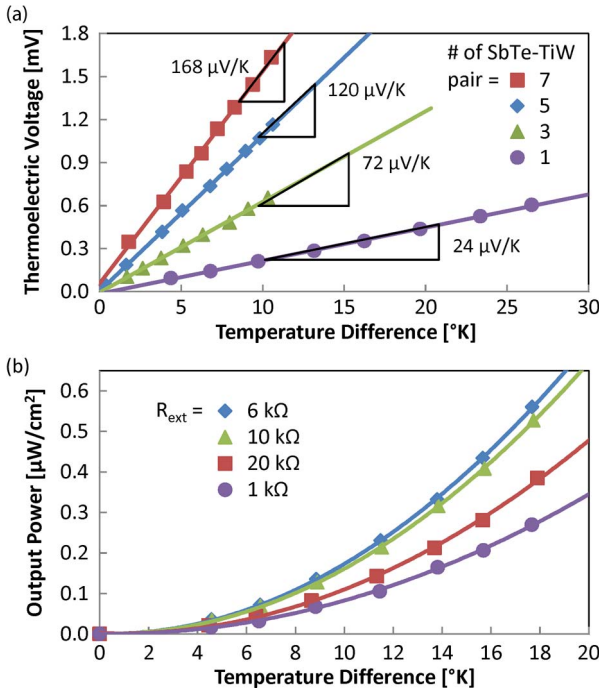

Fig. 4. (a) Thermoelectric voltage measurements with a varying number of thermocouple pairs. The thermoelectric power is consistently measured to be 24 μV/K per SbTe–TiW pair. (b) TEG by a single SbTe–TiW pair for various load resistors with the internal resistance 6 kΩ. Impedance matching produces the maximum output power.

gradient of 18 K. The power generation on the SOI substrate benefits from the proper thermal healing length. Despite the large temperature gradient, the output power is relatively small because the SbTe and TiW are weak thermoelectric materials. The TEG performance can be improved with novel thin-film materials and by further improving the temperature control.

IV. Conclusion

This letter has presented the SOI substrate as a suitable platform for characterizing the thermoelectric power of novel thin-film materials. Control of the thermal healing length, by varying the SOI layer thicknesses, optimized the temperature distribution across the thermoelectric materials. The large thermal healing length enabled the *in situ* IR microscopy, which would be particularly useful for temperature-dependent measurements. Our measurements of the thermoelectric voltage and the TEG output show the feasibility of SOI-based TEG devices as on-chip power supply. Compared to free-standing membranes, the SOI substrates may achieve smaller temperature gradient but are mechanically much more stable and do not require underetching. Novel self-powered chips and circuits could significantly reduce microfabrication complexity and cost by using the SOI substrate design presented here.

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