THERMAL CONDUCTIVITY AND BOUNDARY RESISTANCE MEASUREMENTS OF GeSbTe AND ELECTRODE MATERIALS USING NANOSECOND THERMOREFLECTANCE

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ABSTRACT

Phase change memory (PCM) uses rapid heating and cooling to induce switching in sub-micron memory cells. The rapid rates of heating and nanoscale dimensions require accurate modeling of thermal transport phenomena in the constituent materials. This motivates improved understanding of the thermal properties of $Ge_2Sb_2Te_5$ (GST) thin films and PCM electrode materials. We report measurements of thermal conductivity and interface resistance of GST and electrode materials by applying nanosecond pump-probe thermoreflectance to multilayer structures of GST-C, GST-TiN, and GST-Ti. We measure the total thermal resistance of the stack from the transient thermal response, separating the intrinsic and boundary resistance terms using a 1-D resistor model of the stack. The intrinsic conductivities for GST are 0.20 W/(m K) for GST-C, 0.33 W/(m K) for GST-TiN, 0.27 W/(m K) for low temperature deposited GST-Ti, and 0.69 for high temperature deposited GST-Ti. The thermal boundary resistances are 27.5 m^2K/GW for GST-C, 5.2 m^2K/GW for GST-TiN, 49.8 m^2K/GW for low temperature GST-Ti, and 11.4 m^2K/GW for high temperature GST-Ti.

KEY WORDS: GeSbTe, phase change memory, multilayer thin film, thermal interface resistance, thin films, transient thermoreflectance

NOMENCLATURE

C	volumetric specific heat, J/(m^3 K)
d	diameter, m
I	intensity, W/m^2
k	thermal conductivity, W/(m K)
$\dot{q}$	heat flux, W/(m^2 K)
R	thermal resistance, m^2 K/GW
T	temperature, K
t	thickness, m
z	position, m

Subscripts

GST	intrinsic property of GeSbTe
C	intrinsic property of carbon
elec	intrinsic property of electrode
r	reflected
Ti	intrinsic property of titanium
TiN	intrinsic property of titanium nitride
trans	intrinsic property of transducer
sub	intrinsic property of substrate
x-y	interface between materials “x” and “y”

Superscripts

LT	low temperature deposited
HT	high temperature deposited

INTRODUCTION

Increasing the data storage density of magnetic hard drive technology is becoming more difficult due to the rising magnetic field densities required. Future hard drives will require new methods of data storage with bit sizes on the order of tens of nanometers and data stability for millions of cycles [1]. Phase Change Memory (PCM) is a promising new non-volatile memory technology that addresses these challenges by offering scalability down to nanometer bit sizes, bit stability during power loss, and long memory cycling life. Phase change materials, first observed by Ovshinsky in 1968, are capable of rapidly switching between amorphous and crystalline phases via joule heating [2]. The amorphous-crystalline transition is the ‘set’ operation, and the reverse is called ‘reset’. PCM cells perform the set operation by rapidly heating the bit above the glass temperature, and allowing it to cool over a period of ~100 ns. The cell resets into the amorphous phase by melting the phase change material and rapidly quenching over a ~10ns time period (fig. 1).

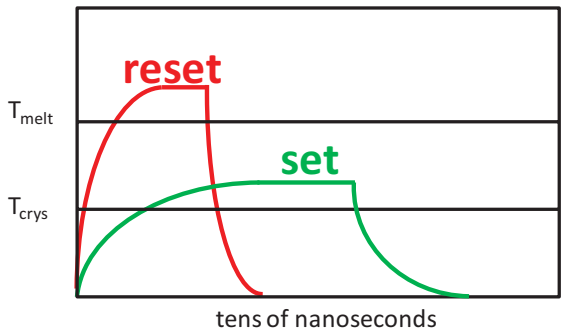

Fig. 1 Set and reset operations for a phase change cell.

There are many ways to implement this style of data storage using both non-contact and contact methods. In non-contact PCM, a laser rapidly heats and quenches a bit on an optical

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disc, using the phase-dependent reflectance contrast to store data. Contact-based PCM utilizes Joule heating in an electrode and/or phase change material to heat the cell (fig. 2). More complex forms of contact PCM cells have been demonstrated by IBM's Millipede structure, which utilizes heated probe tips to locally write and read individual bits [3]. In order to differentiate between the set and reset states of the bit, the electrical resistance of each phase must be dissimilar. The goal of PCM design thus becomes the creation of cells with distinct set and reset resistances, as well as minimized write times, maximum reliability, and maximum bit density. Commonly known phase change materials exhibit well-known and low thermal conductivities.

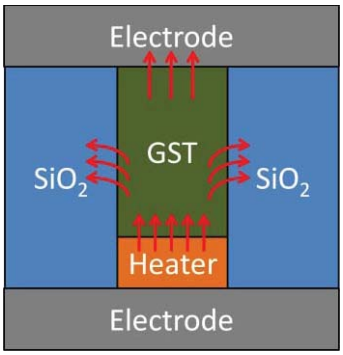

Fig. 2 Cross-sectional view of an electrically switched PCM cell. The arrows indicate direction of heat flow in the device.

$Ge_2Sb_2Te_5$ (GST) is the most common phase change material in PCM devices. This material offers a large difference in electrical conductivity between the amorphous and crystalline phases [4]. The intrinsic thermal conductivity is well-characterized and stable up to 10^5 cycles [5]. The crystallization kinetics of GST allow phase change to occur at nanosecond timescales with a temperature rise ~100 ^oC. These crystallization properties are well-documented. Senkader and Wright demonstrated numerical models of crystal nucleation and growth in a PCM cell [4], [6]. Zhou [4], Kooi et al [7], and Kolobov et al [8] presented results on measurements of crystallization rates in GST and other PCM materials.

As device dimensions reduce to tens of nanometers to accommodate greater data density, the thermal resistance of the interfaces becomes comparable to the volumetric resistances. [9]. TBR tends to be in the range of 1 to 100 m^2K/GW for most material boundaries. Assuming the TBR of GST-SiO_2 is roughly 10 m^2K/GW and K_{SiO2} ~ 1.4 W/mK, the boundary acts like a layer of SiO_2 with effective thickness t ~ 10 nm. As such, it is essential to characterize the TBRs between GST and electrode materials to accurately model devices of interest.

Previous Work

Early thermal boundary resistance (TBR) measurements were performed by Kapitza during his experiments on thermal conduction between Cu and liquid He [10]. The first attempt to model this resistance interpreted phonon transmission at a material boundary as being similar to photon transmission and reflection between materials with different refractive indices. This Acoustic Mismatch Model (AMM) indicated that transmission of phonons was dependent upon the sound speed and density of the interacting materials. However, this model assumes a perfect planar interface, and is only accurate at temperatures below 10K, when phonon wavelength is much greater than the boundary roughness [11]. Swartz and Pohl extended this model to higher temperatures, where higher frequency phonons scatter diffusely on defects and the rough material boundary [11]. However, this model is also limited, often under-predicting boundary resistance. As a result, experimental determination of TBR is imperative.

Using AMM, the TBRs between a-GST and electrode materials are 0.03 m^2K/GW for carbon, 2.0 m^2K/GW for titanium, and 0.9 m^2K/GW for titanium nitride at 300 K. The corresponding resistances for c-GST are 0.07, 0.88, and 1.9 m^2K/GW. Studies on the TBR between GST and electrode materials show data that exceed these estimates [12], implying that interfacial effects dominate over acoustic mismatch.

For PCM devices, Reifenberg et al. [9] demonstrated the importance of thermal boundary resistance. Yang et al. and Reifenberg et al. measured the dependence of thermal conductivity on the stoichiometry and thickness of GST, determining that concentration of Te and film height can drastically change the thermal properties of the material [13], [14]. Lyeo et al measured the conductivity of GST with Time Domain Thermoreflectance Thermometry [15], yielding ~0.19 W/(m K) for a-GST, ~0.57 W/(m K) for c-GST, and ~1.58 W/(m K) for h-GST. Giraud et al measured the intrinsic thermal conductivity of GST insulated with ZnS:SiO_2 using the 3ω method [16]. They obtained thermal conductivities of ~0.24 W/(m K) for a-GST and ~0.29 W/(m K) for c-GST. Due to the unique crystallographic nature of the authors' samples, along with their decision to neglect GST-ZnS:SiO_2 TBR and spreading resistance, the measured thermal conductivities are low compared to other literature data.

Thermal boundary resistance depends on the interface qualities and phonon properties of each material. Electron-phonon interactions may contribute at metal/nonmetal interfaces [11]. Approaching the Debye temperature, the effect of the phonon acoustic spectra and electron-phonon interaction on TBR is small compared to the effect of interface properties, such as grain boundaries, impurities, and surface defects. These latter properties depend on deposition method.

For this study, multi-layer stacks consisting of varying thicknesses of GST on electrode materials are prepared. Measuring the thickness dependence of the thermal resistance of the multi-layer GST-electrode material stacks provides a means to separate the intrinsic GST thermal conductivity from the GST-electrode TBR. A reflective layer of Ti forms a capping layer for all the samples. Nanosecond thermoreflectance measurements determine the total thermal resistance of the GST-electrode stacks. The results demonstrate the importance of sample processing in controlling thermal boundary resistance. This data is essential for construction of future thermal models of PCM devices.

EXPERIMENTAL METHOD

Sample Preparation

The multilayer samples were prepared by physical vapor deposition (PVD). Each sample consists of alternating layers of GST and one electrode material: Ti, TiN, or C. The GST layers vary in thickness between ~50 nm and 150 nm. The electrode materials have constant thickness targeted ~5 nm. The GST-C and low temperature $(GST\text{-}Ti)^{LT}$ samples were deposited at room temperature, leaving the GST in the as-deposited phase. The TiN layers in the $(GST\text{-}TiN)^{HT}$ stacks were reactively sputtered in a nitrogen-containing ambient environment using a titanium target. Electrical resistivity measurements indicate the GST films in the $(GST\text{-}TiN)^{HT}$ films partially crystallize into the FCC phase due to the elevated deposition temperature. The high temperature $(GST\text{-}Ti)^{HT}$ film is deposited above 135°C. Electrical resistivity measurements indicate the GST films in the high temperature $(GST\text{-}Ti)^{HT}$ stacks are deposited in the FCC phase. The thicknesses of all samples are confirmed using scanning electron microscope (SEM) images (fig. 3). Tables 1 and 2 report stack thickness and deposition temperatures.

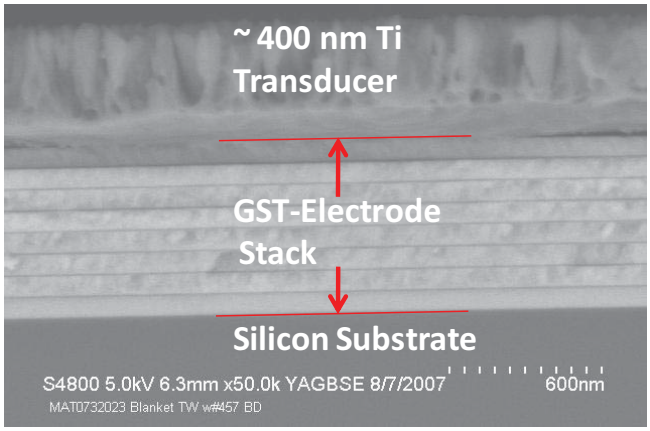

Fig. 3 Example GST-Electrode multilayer sample. Total stack thickness is ~ 680 nm, with a 400 nm Ti transducer layer.

Table 1. Thickness of GST and number of periods of GST-Electrode measured by SEM.

Sample	Stack 1 (nm) (# periods)	Stack 2 (nm) (# periods)	Stack 3 (nm) (# periods)
$(GST\text{-}C)^{a}$	305 (6)	649 (6)	930 (6)
$(GST\text{-}C)^{b}$	643 (4)	639 (8)	629 (10)
$(GST\text{-}TiN)^{HT}$	270 (6)	520 (6)	680 (6)
$(GST\text{-}Ti)^{LT}$	322 (6)	633 (6)	970 (6)
$(GST\text{-}Ti)^{HT}$	335 (6)	623 (6)	890 (6)

Table 2. Chamber temperature during deposition of GST and electrode materials.

Sample	GST Dep Temp (°C)	Electrode Dep Temp (°C)
$(GST\text{-}C)^{a}$	25	not regulated
$(GST\text{-}C)^{b}$	25	not regulated
$(GST\text{-}TiN)^{HT}$	135	not regulated
$(GST\text{-}Ti)^{LT}$	25	not regulated
$(GST\text{-}Ti)^{HT}$	135	not regulated

Nanosecond Thermoreflectance

Nanosecond thermoreflectance thermometry characterizes the thermal properties of the sample structures by optically measuring their transient thermal response to nanosecond pulse heating. A high-power 532 nm Nd:YAG pump laser heats a 10 mm^2 area on the surface of the sample with a 6 ns pulse at a repetition rate of 10 Hz. (fig. 4). Assuming total absorption of a 6 mJ pulse with no heat dissipation, the maximum temperature rise of the Ti transducer is ~ 10 K.

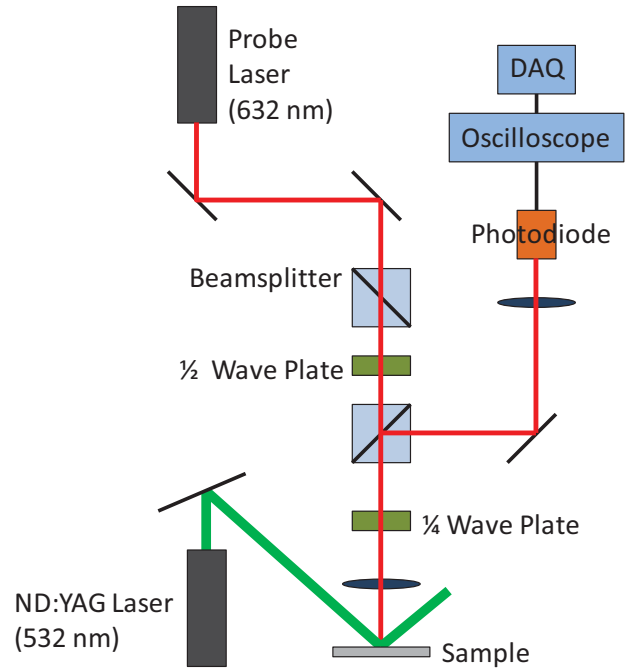

Fig. 4 Top view of the nanosecond thermoreflectance setup.

A 650 MHz photodiode and amplifier measures the reflected intensity of a coincident 632 nm CW probe beam during a 20 µs temporal window after the pump pulse. The change in reflected laser intensity scales linearly with the change in temperature of the metal film according to:

$$\frac{\Delta I_r}{I_{r0}} = c_{tr}\,\Delta T \qquad (1)$$

where c_{tr} is a material-dependent thermoreflectance constant and I_r is the reflected signal intensity [17], [18], [19]. The voltage signal, captured with an oscilloscope, tracks the

relative temperature decay of the Ti transducer with a temporal resolution of 20 ns. Since the measurement technique and non-dimensional heat diffusion equation are both linear with temperature, the thermal properties of the stack can be determined without knowledge of c_{tr}. The accuracy of the nanosecond setup was confirmed by observing the decay time of a TiN transducer layer on a quartz substrate. Figure 5 shows the experimental data and a corresponding analytical fit using the known properties of these materials.

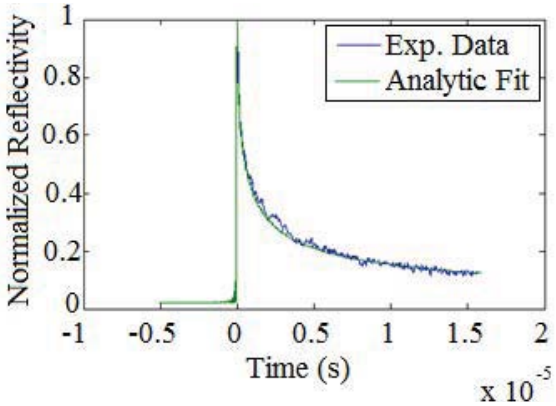

Fig. 5 Results for the TiN on SiO_2 on Si calibration sample.

THEORETICAL

Data Fitting

The thermal conductivities of the stacks are extracted using a least squares fit of a solution of the three dimensional radially-symmetric heat diffusion equation for a multi-layered stack in response to a 6 ns surface heating pulse [20], [12]. Ambient temperature for the fit is 30 °C. Small changes in ambient temperature do not affect the fitting results because the thermal properties of the samples are not strong functions of temperature. The boundary condition between each layer is:

$$T_i(z_0) = T_{i+1}(z_0) + \frac{R_{i,i+1}}{\dot{q}_i} \qquad (2)$$

where $R_{i,i+1}$ is the thermal boundary resistance. In this case, a single layer which includes both the interface and volumetric contributions to the thermal resistance models the behavior of the GST-Electrode stack. The data are fit with a single effective thermal conductivity of this layer. The heat capacity of GST is given by [21]. Although the solution takes into account thermal spreading, this effect is negligible and the heat transfer is one dimensional since the pump beam waist is significantly larger than the maximum thermal diffusion depth during the measurement. Since heat transfer is one dimensional, effective stack resistance can be interpreted in terms of a series of thermal resistances (fig. 6).

A trace is taken at ten different locations on the wafer. Averaging the fitted thermal conductivity from each trace reduces the effects of noise and film thickness variation. The standard deviation of thermal conductivity between individual traces makes up the error bars.

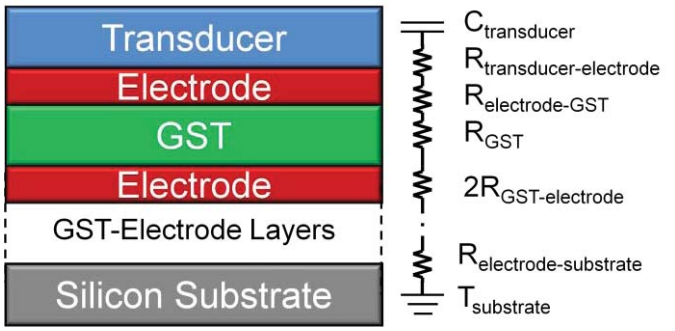

Fig. 6 Diagram of a 1-D multilayer resistance model. The intrinsic resistance of the transducer is negligible.

Stack Resistor Model

Within this 1-D framework, the thermal resistance of the stack increases linearly with GST thickness. The slope of stack resistance versus GST thickness determines the intrinsic GST conductivity. The zero-thickness value of total resistance becomes the total boundary resistance of the stack. Assuming that each boundary possesses the same resistance and that the electrode layers are thin enough so that their intrinsic resistance is negligible, one may divide the zero-thickness thermal resistance by the total number of boundaries to determine the individual GST-electrode material TBR. The total resistance of the stack becomes:

$$R_{total} = \frac{t_{GST}}{k_{GST}} n + 2R_{GST-elec}(n+1) + \frac{t_{elec}}{k_{elec}}(n+1) + R_{trans-elec} + R_{elec-sub} \qquad (3)$$

where t is material thickness, k is intrinsic thermal conductivity, and n is the number of layers in the stack. The thermoreflectance traces are fit starting from 100 ns after the peak, at which point the solution is insensitive to the transducer-electrode TBR. Further, since the characteristic decay time of the stack is significantly larger than the timescale of the measurement, the solution is also insensitive to the electrode-substrate TBR. Finally, since t_{elec} is small, the intrinsic electrode resistance can usually be neglected.

For the GST-C samples, the intrinsic resistance of the electrode material is too large to neglect even at such a small thickness. Assuming a thickness of 5 nm and a conductivity of 0.2 W/(m K), yields a volumetric resistance of 25 m^2K/GW, which is on the order of most TBRs. Furthermore, the carbon thickness is difficult to determine due to its small size. Since each group of electrode samples is produced in the same batch run, one may assume that the electrode layer thickness is unknown but constant. As a result only the slope of the resistance-thickness curve is reliable. This determines only the intrinsic GST conductivity. To extract TBR, we designed a set of samples with varying numbers of GST-electrode periods in each stack, maintaining a constant total GST material thickness. In this case, we can plot the total thermal resistances of these stacks against the numbers of GST-electrode period and obtain a straight line. The slope of this line determines the sum of GST-C TBR and carbon thermal resistance in each period of the stack.

Since the electrode layers in these samples are thin, there may be significant interdiffusion between the GST and electrode materials. As a result, the interface resistance may be due to both atomic disorder and an abrupt change in material properties [22]. Equation 3 assumes a discernible GST-electrode interface. Cross-sectional SEM data (fig. 3) of the samples demonstrate a noticeable material interface between the GST and electrode layers. There is insufficient resolution to determine the electrode thickness or whether the electrode material forms a distinct interface with the surrounding GST. Since each GST layer sees two electrode boundaries, this analysis assumes two GST-electrode TBRs per layer.

RESULTS

Figures 7 through 10 show the thermoreflectance results. For Carbon, TiN, and low temperature deposited $(GST\text{-}Ti)^{LT}$, the intrinsic GST conductivity ranges from 0.20 to 0.33 W/(m K). This is within the conductivity values reported in previous studies for amorphous GST [14], [15], [16]. The GST thermal conductivity values in the $(GST\text{-}Ti)^{LT}$ and $(GST\text{-}TiN)^{LT}$ stacks, are slightly higher than previous reports, indicating that a small degree of crystallization may be taking place during the deposition process. The intrinsic conductivity of GST for the $(GST\text{-}Ti)^{HT}$ sample is 0.69 W/(m K), higher than the results reported for the FCC phase. This suggests that partial HCP crystallization may be occurring [13], [14].

The GST-C TBR plus the intrinsic carbon resistance is 40 m^2K/GW, as depicted in figure 8. Taking into account the reported 5 nm of carbon, this gives a TBR of 27.5 m^2K/GW, with a potential error of ±6 m^2K/GW due to uncertainty in carbon thickness [23]. This TBR corresponds to ~5 nm of carbon. The $(GST\text{-}Ti)^{LT}$ TBR is 49.8 m^2K/GW, equivalent to ~1000 nm of Ti. This is reduced to 11.4 m^2K/GW for $(GST\text{-}Ti)^{HT}$, equivalent to ~200 nm of Ti. The $(GST\text{-}TiN)^{HT}$ TBR is lowest of all, with 5.2 m^2K/GW, equivalent to ~150 nm of TiN. Table 3 reports the collected data.

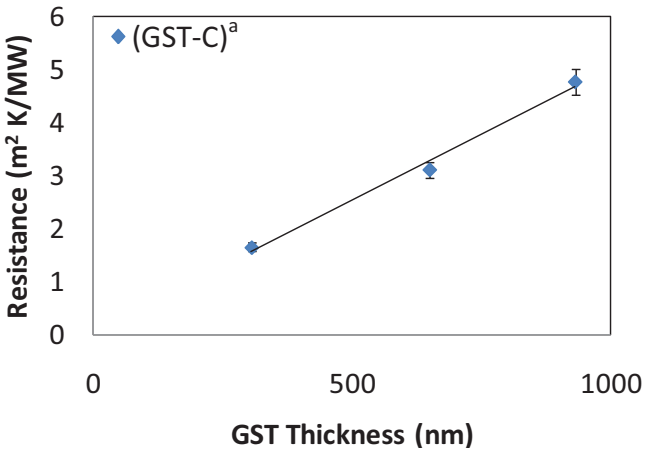

Fig. 7 Plot of total stack resistance versus thickness for GST-Carbon sample a. Slope indicates GST conductivity is 0.20 W/(m K)

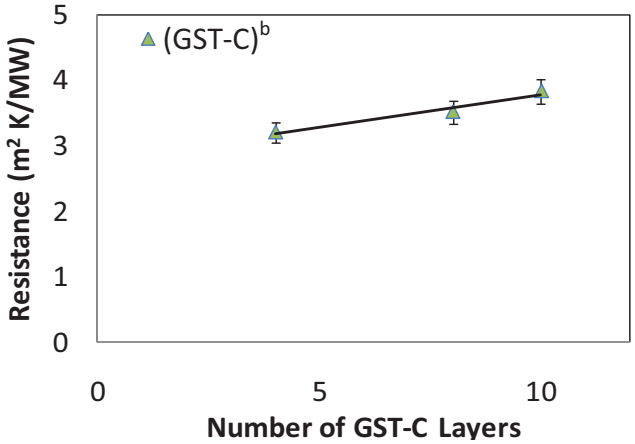

Fig. 8 Plot of total stack resistance versus thickness for GST-Carbon sample b. Slope indicates GST-Carbon TBR + Carbon resistance = 40 m^2K/GW.

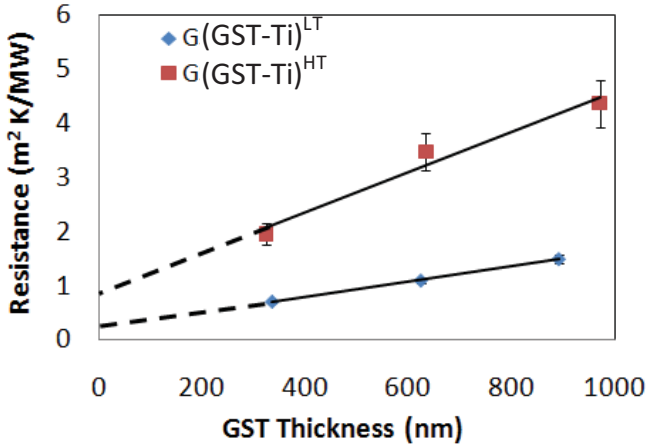

Fig. 9 Plot of total stack resistance versus thickness for GST-Ti and high temperature deposited GST-Ti. Slopes indicate GST conductivities are 0.27 and 0.69 W/(m K) respectively. GST-Ti TBRs are 49.8 and 11.4 m^2K/GW respectively.

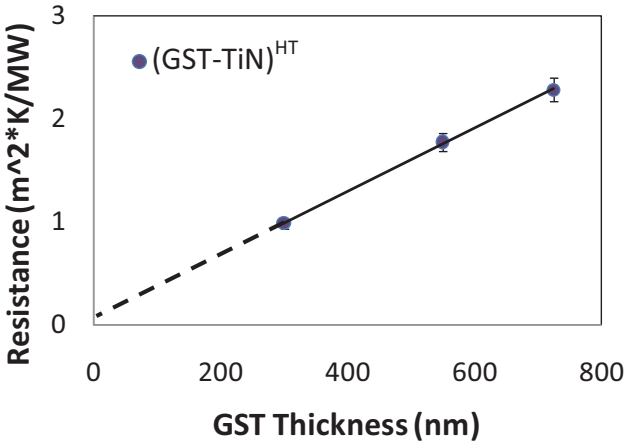

Fig. 10 Plot of total stack resistance versus thickness for $(GST\text{-}TiN)^{HT}$. Slope indicates GST conductivity is 0.33 W/(m K). $(GST\text{-}TiN)^{HT}$ TBR is 5.2m^2K/GW

Table 3. Collected GST-Electrode results. a) Constant layer count. b) Constant stack thickness

Electrode Material	Intrinsic GST Conductivity (W/(m K))	TBR (m^2K/GW)
(GST-C)[a]	0.20 ± 0.01	N/A
(GST-C)[b]	N/A	27.5 ± 6
(GST-TiN)^{HT}	0.33 ± 0.017	5.2 ± 0.25
(GST-Ti)^{LT}	0.27 ± 0.014	49.8 ± 2.5
(GST-Ti)^{HT}	0.69 ± 0.035	11.4 ± 0.6

The intrinsic conductivity of GST in the (GST-C)[a] stack is the lowest of all the samples. Due to the low temperature deposition procedure for carbon, no crystallization takes place in the GST. Since the GST-C TBR is moderately high compared to other material interface resistances, and since the intrinsic thermal resistance of carbon is high, a carbon electrode can impede the loss of heat from a PCM cell, resulting in a large thermal decay time. This may lower the programming current necessary to switch the device.

The (GST-TiN)^{HT} sample has higher intrinsic GST conductivity due to the higher deposition temperature. This most likely causes partial formation of the FCC crystalline phase in the GST. High temperature deposition processes are acceptable because the device can be reset. Furthermore, the (GST-TiN)^{HT} TBR is very small, resulting in a small thermal decay time. Reifenberg et al. report a room temperature (GST-TiN)^{HT} TBR of ~ 26 m^2K/GW for samples of GST between two layers of TiN [12]. This measurement, performed using picosecond time-domain thermoreflectance (TDTR), utilized samples with TiN thickness greater than 10 nm. These thicker TiN films may possess a higher degree of surface roughness, resulting in a larger TBR than reported in this paper. The high boundary conductance between GST and TiN implies a higher programming current necessary to switch the device.

For the (GST-Ti)^{LT} stack, the intrinsic conductivity of the GST is slightly higher than expected for amorphous GST, indicating a small amount of crystallization may be occurring. The (GST-Ti)^{HT} exhibits partial HCP crystallization. This is not an issue for device fabrication since the cell switches easily between the amorphous and crystalline states. The difference in TBR between the (GST-Ti)^{LT} and (GST-Ti)^{HT} stacks demonstrates the importance of deposition method on device performance. Depending on the temperature of deposition, the thermal decay time and programming current of the device change. A higher deposition temperature results in a lower thermal decay time for the device, implying a higher programming current is necessary. Accordingly, PCM designers must be careful to choose fabrication processes that will result in devices with desirable thermal properties.

SUMMARY AND CONCLUSIONS

This paper reports intrinsic conductivities and thermal boundary resistances for GST and various electrode materials. Since the latter properties are highly dependent on the deposition method of the films, sample fabrication mimicked that of an actual device as closely as possible. Intrinsic amorphous GST conductivities range from 0.2 to 0.33 W/(m K). For high temperature deposition, the intrinsic GST conductivity is 0.69 W/(m K). TBRs range from 5.2 to 49.8 m^2K/GW. High temperature deposition significantly reduces the TBR of GST-Ti. The results of this paper are a valuable addition to the collected work on GST conductivity and thermal boundary resistance. With this data, more accurate thermal models of PCM cells are now possible.

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