Thermal Phenomena in Nanoscale Transistors

Eric Pop
Department of Electrical Engineering,
Stanford University,
Stanford, CA 94305

Kenneth E. Goodson
Department of Mechanical Engineering,
Stanford University,
Stanford, CA 94305
e-mail: goodson@stanford.edu

As CMOS transistor gate lengths are scaled below 45 nm*, thermal device design is becoming an important part of microprocessor engineering. Decreasing dimensions lead to nanometer-scale hot spots in the drain region of the device, which may increase the drain series and source injection electrical resistances. Such trends are accelerated with the introduction of novel materials and nontraditional transistor geometries, like ultra-thin body, surround-gate, or nanowire devices, which impede heat conduction. Thermal analysis is complicated by subcontinuum phenomenan including ballistic electron transport, which reshapes the hot spot region compared with classical diffusion theory predictions. Ballistic phonon transport from the hot spot and between material boundaries impedes conduction cooling. The increased surface to volume ratio of novel transistor designs also leads to a larger contribution from material boundary thermal resistance. In this paper we survey trends in transistor geometries and materials, from bulk silicon to carbon nanotubes, along with their implications for the thermal design of electronic systems.* [DOI: 10.1115/1.2188950]

1 Introduction

The technological revolution that started with the introduction of the transistor just over half a century ago is without parallel in the way it has shaped our economy and our daily lives. The current trend toward nanoscale electronics is expected to have a similar impact into the third millennium. Commercial microprocessors are already available with transistors whose smallest lateral feature size is less than 100 nm and the thinnest material films are below 2 nm, or only a few atomic layers thick. Such miniaturization has led to tremendous integration levels, with a hundred million transistors assembled together on a chip area no larger than a few square centimeters. Integration levels are projected to reach the gigascale as the smallest lateral device feature sizes approach 10 nm. The most often cited technological roadblock of this scaling trend is the "power problem," i.e., power densities, heat generation, and chip temperatures reaching levels that will prevent the reliable operation of the integrated circuits. Chip-level power densities are currently on the order of 100 W/cm^2, and if the rates of integration and miniaturization continue to follow the ITRS (International Technology Roadmap for Semiconductors) guidelines [1], the chip-level power density is likely to increase even further [2], as illustrated in Fig. 1. Higher power densities will quickly drain batteries out of portable devices and render most advanced, future electronics unusable without significant cooling technology, or fundamental shifts in design. The situation is compounded by millimeter-scale hot spots on the chip, i.e., localized regions of higher heat generation rate per unit area, hence higher temperatures (e.g., near the clock) [3].

While the total heating rate of microprocessor chips has received much attention [4], a different thermal management challenge faces device and circuit designers at nanometer length scales, within individual transistors. Novel, complicated device geometries tend to make heat removal more difficult, and most new materials being introduced in device processing have lower thermal conductivities than bulk silicon (Fig. 2 and Table 1). In addition, subcontinuum effects must be taken into account in the thermal modeling of devices with dimensions less than the electron (charge carrier) or phonon (heat carrier, i.e., quantized lattice vibration) mean free paths. Such effects include quasiballistic electron and phonon transport in the transistor "hot spot" region of tight electron-phonon coupling. Nonlocal transport conditions in this vicinity cause such hot spots to be spatially displaced and to have a higher temperature rise compared with classical heat diffusion theory predictions [5,6]. Also, the thermal conductivity of semiconductor films thinner than the phonon mean free path is significantly reduced by phonon confinement and boundary scattering.

In this paper we review the thermal management issues associated with nanometer-scale transistors. In the first section we introduce a novel method for computing heat (phonon) generation rates in semiconductors, with the aid of Monte Carlo simulations. In the next section we discuss the impact of various material choices on the heat transport characteristics of future-generation transistors. The remainder of the paper is dedicated to an overview of heat transfer issues in five types of semiconductor transistors (bulk silicon, thin film devices, germanium devices, nanowires, and nanotubes), with particular emphasis on the nonclassical, subcontinuum aspects of their behavior.

2 Heat Generation

Modern device technologies already operate at length scales on the order of the electron and phonon mean free paths (approximately 5–10 and 200–300 nm in bulk silicon at room temperature, respectively [7,8]), and future technologies are going to forge deeper into this subcontinuum regime. Nearly ballistic conditions are expected to dominate both electron (current) and phonon (heat) transport, leading to a strong nonequilibrium between the energy carriers at nanometer length scales. The electron-phonon interaction is neither energetically nor spatially uniform and the generated phonons have widely varying contributions to heat transport: Optical phonons make virtually no contribution to the thermal conductivity, which is dominated by acoustic phonon transport [8,9].

In the context of a transistor, the applied voltage leads to a lateral electric field that peaks near the device drain (Fig. 5). This field accelerates the charge carriers (e.g., conduction band electrons in an n-MOSFET) that gain energy, therefore "heating up." Electrons can scatter with each other, with lattice vibrations (phonons), interfaces, imperfections, or impurity atoms. Of these, electrons only lose energy by scattering with phonons, conse-

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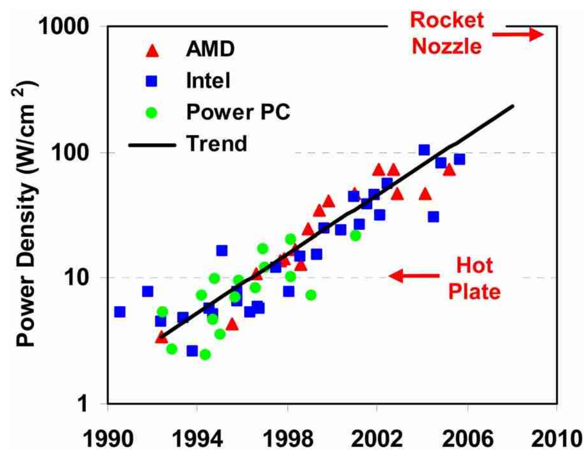

Fig. 1 Trends of on-chip power density for the past 10+ years. Note the vertical axis is logarithmic and the horizontal one (years) is linear. By comparison, typical power densities for a hot plate and a rocket nozzle are listed, while the surface of the sun puts out approximately 7000 W/cm^2. The solid line marks an exponential trend. (Data compiled by F. Labonte, Stanford.)

quently heating up the lattice (i.e., Joule heating). Other scattering mechanisms are all considered elastic, only affecting the electron momentum [7]. The lattice absorbs the extra electron energy, heats up to a higher temperature (T), and in turn affects the electronic transport properties of the material: The electron mobility in bulk (undoped) silicon decreases approximately as $T^{-2.4}$ around room temperature. When other, less temperature sensitive scattering mechanisms also come into play, the electron mobility is more weakly dependent on temperature: It decreases as $T^{-1.7}$ in highly doped silicon and $T^{-1.4}$ in ultrathin silicon films [10].

In silicon, as in most semiconductors, high field Joule heating is typically dominated by optical phonon emission. Optical phonons are slow and they make virtually no contribution to heat transport. Rather, they decay into the faster acoustic modes, which carry the energy away from the hottest regions. Optical to acoustic decay times are relatively long (on the order of picoseconds [11]) compared to the electron-phonon scattering time (tenths of picoseconds). If the generation rate of optical modes due to Joule heating from current flow is higher than their rate of decay into acoustic modes, a phonon energy bottleneck is created and the optical mode density can build up over time, directly affecting electron transport.

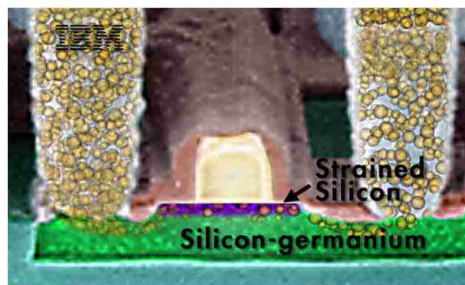

Fig. 2 False-color Transmission Electron Microscopy (TEM) cross-section of a future-generation strained silicon-on-insulator (SSOI) transistor. Image courtesy IBM.

Table 1 Thermal conductivities of a few materials used in device fabrication. Phonon boundary scattering significantly reduces the thermal conductivity of a 10 nm thin silicon film. Note that phonons are responsible for the thermal conductivity of all dielectric materials listed, but electrons are the heat carriers in silicides, which are metals.

Material	Thermal Conductivity ($Wm^{-1} K^{-1}$)
Si (bulk)	148
Ge (bulk)	60
Silicides	40
Si (10 nm)	13
$Si_{0.7}Ge_{0.3}$	8
SiO_2	1.4

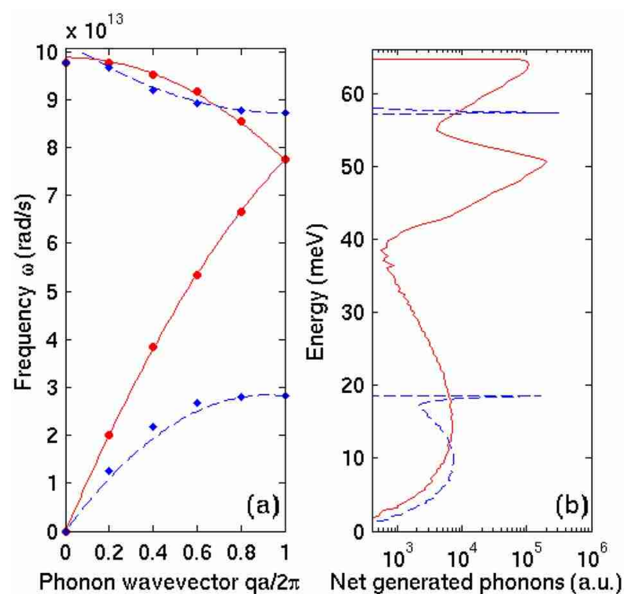

Fig. 3 Phonon dispersion in the (100) direction of silicon (*a*) and computed net (emission minus absorption) phonons generated by Joule heating (*b*). The symbols in (*a*) are from neutron scattering data and the lines are a quadratic fit [14]. Solid lines are for longitudinal, and dashed lines are for transverse phonons. Optical modes are above and acoustic modes have energies below approximately 50 meV, respectively. Note the vertical axes are matched ($E=\hbar\omega$) to facilitate comparison of the dispersion and generated modes.

The volumetric Joule heating rate in the context of a device simulator is typically captured as the dot product of the electric field (**E**) and current density (**J**) [5,12]. Unfortunately, this approach does not account for the *microscopic* nonlocality of the phonon emission near a strongly peaked electric field region, such as the drain of a transistor. Although electrons gain most of their energy at the location of the electric field peak, they typically travel several mean free paths before releasing all of it to the lattice, in decrements of (at most) the optical phonon energy. In silicon transistors, for example, electrons can gain energies that are a significant fraction of an eV, while the optical phonon energy is only about 60 meV. Assuming an electron velocity of 10^7 cm/s (the saturation velocity in silicon) and an electron-phonon scattering time around 0.05–0.10 ps in the high-field region, the electron-phonon mean free path is then on the order of 5–10 nm. The full electron energy relaxation length is therefore even longer, on the order of several mean free paths. While such a small discrepancy may be neglected on length scales of microns, or even tenths of a micron, it must be taken into account when considering lattice heating on length scales of 10 nm, as in a future generation transistor. The highly localized electric field in such devices leads to the formation of a nanometer-sized hot spot in the drain region, that is spatially displaced (by several mean free paths) from continuum theory predictions. In addition, the $\mathbf{J}\cdot\mathbf{E}$ formulation of the Joule heating also does not differentiate between electron energy exchange with the various phonon modes, and does not give any

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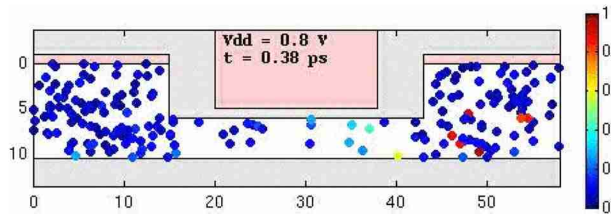

Fig. 4 Snapshot of electron transport in a future-generation thin-body silicon-on-insulator (SOI) device simulated with the Monte Carlo code MONET [13,15]. The color scale is the electron energy in eV and the device dimensions are in nm.

spectral information regarding the types of phonons emitted.

A Monte Carlo (MC) simulation method was recently introduced to compute subcontinuum and phonon mode-specific heat generation rates, with applications at nanometer length scales [13,14]. Both the electron bands and the phonon dispersion can be modeled analytically as ellipsoids and quadratics, respectively. This is a good approximation for devices operating at voltages below the silicon band gap (1.1 V), such as those of future technologies, and it enables a significantly faster code that is easier to implement and debug [15]. Impact ionization is suppressed at sub-band gap voltages, so it can be safely ignored. Inelastic scattering with all intervalley, as well as intravalley phonons was incorporated, as given by scattering selection rules and by the phonon dispersion. Particular care was taken to treat the acoustic phonon interaction inelastically, including the phonon dispersion. An isotropic, analytic fit to the dispersion relation (see Fig. 3(*a*)) was also used when computing the final state after scattering with both optical and acoustic phonons, satisfying momentum and energy conservation.

The phonon emission and absorption events during a simulation run are tallied and full heat generation statistics can be collected. Fig. 3(*b*) shows the net (emission minus absorption) generated phonons during a typical simulation of current flow and Joule heating in a silicon resistor with a constant 50 kV/cm applied electric field. The shape of the generated phonon distribution approximately follows the density of states, while the specific phonons involved are given by the various scattering selection rules [16]. The area under each peak is proportional to the square of the coupling constant (deformation potential) of the respective electron-phonon interaction, and is a measure of the strength of each scattering type [13,17]. The broadening of the phonon generation peaks occurs when energetic electrons, farther away from the conduction band minima in the Brillouin zone, are allowed to scatter with phonons outside those strictly dictated by the geometrical selection rules. This is a direct consequence of using a continuous analytic representation of the phonon dispersion in selecting the final states. The resulting phonon generation spectra can be used as inputs for molecular dynamics [18] or phonon Monte Carlo simulators [9], and they offer a comprehensive look at the complexity of Joule heating in silicon. The code can also be run in the context of a realistic device design, collecting electron transport and heat generation information across the simulation domain (Fig. 4).

Similar heat generation statistics could also be evaluated for different materials (e.g. germanium) as well as for strained or confined nanostructures. Restricted dimensions may lead to confined phonon modes [19], but the electron-phonon scattering rate can be recomputed, taking into account the modified phonon dispersion. This can be done efficiently as long as the phonon dispersion is recast as a set of analytic functions (e.g., polynomials). This Monte Carlo tool (named MONET) will be available through the NCN Computational Nanohub [20].

3 Material Thermal Properties

Traditional, bulk transistor designs (Fig. 5(*a*)) typically incorporate only a few materials, most notably silicon, silicon dioxide insulators and silicided (e.g., NiSi) contacts. The high thermal conductivity of bulk silicon (148 $\mathrm{W m^{-1} K^{-1}}$) facilitates heat transport from the transistor channel down to the backside of the chip, where it has been traditionally removed with a heat sink.

Advanced, nontraditional device fabrication introduces a number of new materials with lower thermal conductivities. The thermal properties of these materials are therefore expected to play a more significant role in the device design and thermal behavior. Table 1 lists the thermal conductivities of a few materials used in semiconductor device fabrication. Bulk germanium transistors, for example, would suffer from increased operating temperatures due to a substrate thermal conductivity approximately 60% lower than bulk silicon transistors. Strained silicon channel devices (Fig. 5(*b*)) grown on a graded $Si_{1-x}Ge_x$ buffer layer benefit from an increased mobility due to band degeneracy splitting and a lighter effective mass in the strained film. However, their thermal behavior is adversely affected by the lower thermal conductivity of the $Si_{1-x}Ge_x$ alloy layer. The situation is worse for thin body devices grown on a silicon dioxide film. From an electrical point of view, silicon-on-insulator (SOI) devices benefit from lower capacitive coupling with the substrate, and hence increased switching speeds. Thermally, however, they are significantly affected by the very low thermal conductivity of the buried oxide layer, which is about two orders of magnitude less than that of silicon. The thermal conductivity of thin semiconductor films (thinner than the phonon mean free path) is also significantly reduced by phonon boundary scattering. A 10 nm thin silicon film is expected to have a thermal conductivity reduced by an order of magnitude from that of bulk silicon, based on theoretical estimates [21]. Although experimental data for such thin films does not yet exist, this estimate is based on extrapolations to available data [22], and also supported by recently measured reduced thermal conductivities in silicon nanowires [23].

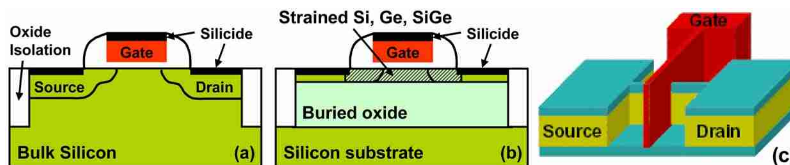

Fig. 5 Evolution of transistor designs from traditional bulk silicon (*a*) to (strained) silicon or germanium on insulator (*b*), to multiple-gate or FinFET devices (*c*). Non-traditional device designs like (*b*) and (*c*) introduce more complicated geometries and lower thermal conductivity materials, making heat removal more difficult. The gate length (currently near 50 nm) is expected to be scaled to the 10 nm range, while the semiconductor film and "fin" thickness of (*b*) and (*c*), respectively, are approximately one third to one half the gate length. Figure (*c*) is from the technology roadmap (ITRS) [1].

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The small dimensions of future device designs also imply a large surface-to-volume ratio (Fig. 5), and hence a stronger effect of material boundary resistance. Few estimates exist on the magnitude of the *thermal* boundary resistance between dissimilar materials (e.g., dielectrics and metals). Some measurements indicate it is on the order of the thermal resistance of a 20 nm thick silicon dioxide film [24], and fairly independent of processing conditions or the specific type of metal and dielectric involved. This is a significant value for nanoscale devices, and very important to understand. As more materials (e.g., high-*k* dielectrics, germanium, various silicides) are introduced in semiconductor processing, there is a growing need to understand the magnitude of boundary thermal resistance and its significance in future nanoscale device behavior. The boundary thermal resistance plays a significant role, for example, when a metal electrode is placed on top of the high-*k* gate dielectric (as expected for threshold voltage control in future technologies) as well as for device metal contacts and interconnects. More measurements are needed in this area, while more available data on thermal boundary resistance would also help toward a better understanding (and modeling) of the atomic scale interaction at the interface between two materials.

4 Bulk Silicon Transistors

The bulk CMOS silicon transistor (Fig. 5(*a*)) has been (and still is) the principal building block of the semiconductor industry for the past 40 years. Thermal transport in bulk transistors has traditionally been modeled in the classical limit, as subcontinuum effects could be neglected for device dimensions larger than the phonon mean free path. As devices are scaled below 100 nm, two subcontinuum effects are expected to play a role in transistor-level thermal transport. The small region of the high electric field near the drain gives rise to a small (only a few tens of nanometers across, and hence much smaller than the bulk phonon mean free path), localized hot spot. This leads to ballistic phonon transport in the vicinity of the heat source and higher temperatures than those predicted by classical diffusion theory [6,25]. In this situation, a solution to the phonon Boltzmann Transport Equation is more accurate than the classical heat diffusion equation [5,26].

The second subcontinuum thermal effect to be expected in ultra-scaled transistors has to do with the nonequilibrium interaction between the generated optical and acoustic phonons. Since nearly stationary optical phonons form the majority of the vibrational modes generated via Joule heating, they tend to persist in the hot spot region until decaying into the faster acoustic modes. This nonequilibrium scenario may become particularly relevant if device switching times approach the optical-acoustic decay times, on the order of 5 ps [11]. A careful transient solution of the phonon populations is necessary to properly account for the nonequilibrium distributions [27,28].

Both subcontinuum effects in bulk nanotransistors are expected to take place in the drain region. Hence, their effect is more likely to be pronounced on device reliability, rather than reducing the device current drive, since the latter is thought to be ultimately determined by the electron injection velocity near the source [29]. However, some indications exist that in the limit of the smallest achievable bulk silicon MOSFETs (10 nm) the optical phonons generated in the drain may reach the device source before decaying into acoustic phonons, and hence directly affect the source injection velocity [6].

5 Thin Body Transistors

Thin body transistors are partially or fully depleted single-gate silicon-on-insulator (SOI) devices, planar (buried gate) dual-gate devices, or vertical FinFETs, as in Figs. 5(*b*) and 5(*c*). They benefit from less capacitive coupling with the substrate, hence higher switching speeds, and more gate control over the channel, hence better turn-on characteristics and threshold voltage control. The subcontinuum phenomena that affect bulk nanotransistors are expected to play a much lower role in thin film transistors. This occurs because the phonon mean free path in the thin film is strongly reduced by boundary scattering to a scale comparable to the device dimensions and the size of the drain-side phonon hot spot.

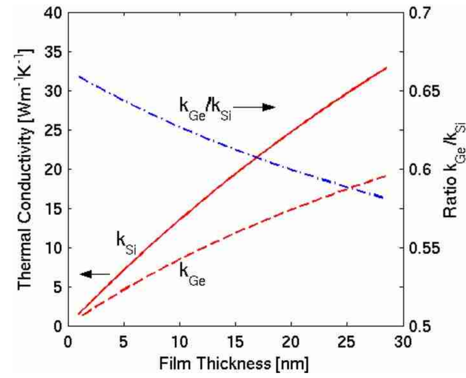

Fig. 6 Estimated reduction in silicon and germanium thin film thermal conductivity due to phonon boundary scattering alone (i.e., no confinement). Thin silicon films suffer from a stronger reduction in thermal conductivity (vs germanium) due to the longer bulk silicon phonon mean free path [30].

However, unlike for bulk devices, the thermal conductivity of the active device region (the thin film body) is much smaller (Fig. 6). In addition, a larger surface area to volume ratio for ultrascaled SOI devices also implies a stronger contribution from the thermal boundary resistance of the various material interfaces. Finally, the very low thermal conductivity of the buried oxide significantly impedes heat transfer toward the substrate. Heat dissipation through the device contacts may play an important role, especially for the smallest, scaled devices. These effects are captured in the thermal resistance model illustrated in Fig. 7. It can be shown that device thermal properties are strongly dependent on the transistor geometry, particularly on the dimensions of the extension length L_{ex} and the raised source/drain height t_{sd} [21]. A shorter L_{ex} and taller t_{sd} are desirable from a thermal point of view, as this choice would minimize the thermal conduction path toward the device contacts. While a taller raised source/drain is also desirable from an electrical point of view (to minimize electrical series resistance), a shorter extension length can lead to significant parasitic gate-to-source capacitance, adversely affecting the switching speed of such a device [30]. Another electrical versus thermal trade-off exists for the thickness of the buried oxide, t_{BOX}: A thinner oxide is desirable from a thermal point of view, although electrically this would lead to higher parasitic coupling capacitance with the substrate. Similar arguments can be made about vertical FinFET devices to show that they generally have better thermal properties owing to their thicker (hence less thermally resistive) body, larger oxide area, and overlapped gate [21]. It is

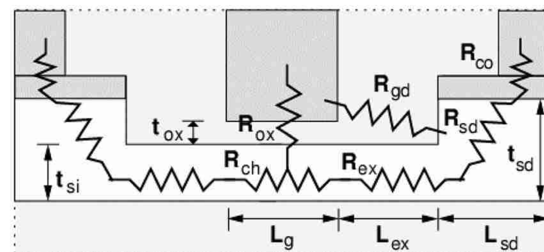

Fig. 7 Thin film transistor thermal resistance model (also see Fig. 5). The dark gray areas represent the metalized gate and contacts, the light gray is the surrounding oxide insulator [21,30].

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clear therefore that both electrical and thermal considerations must be taken into account in the design of ultrascaled future generations of thin body transistors.

It is also important to note the boundary conditions typically used in device-level thermal conduction simulations. With the exception of some heat loss through the gate and the contacts, the top of the device in Fig. 7 is considered adiabatic, since it is covered with oxide. The gate and contacts can be treated as extended surfaces [31] with a certain boundary resistance [30] and heat loss through them can be specifically included [32]. The sides of the device are also considered to be adiabatic by arguments of symmetry, since neighboring devices may be assumed to be equally active and produce comparable power densities. Most of the heat loss occurs through the bottom of the device (and through the buried oxide, in the case of SOI), which can be captured with a lumped thermal resistance of the order 100 K/mW, for a single device of 22 nm gate length. In addition, the chip-level combined thermal resistance from transistor junction to the heat sink is of the order 0.6 K/W [32].

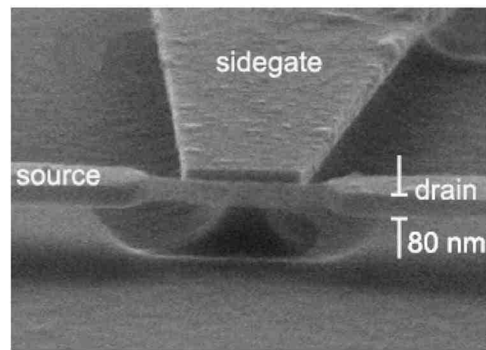

Fig. 8 Suspended silicon nanowire field effect device fabricated with electron beam lithography and a buffered HF underetch [40]. The cross section of the wire is 23×80 nm. The confined dimensions significantly alter both current and heat transport through the wire.

6 Experimental Studies

No experimental studies of self-heating in nanometer-scale (<100 nm) CMOS devices currently exist, to the best of our knowledge. However, several methods have been developed to study the effects of self-heating in larger devices over the past ten years. The approach of Su et al. [31] used gate thermometry to estimate the channel temperature of devices with gate lengths of the order 1 μm, and found a thermal resistance of approximately 10 K/mW for SOI and 1 K/mW for bulk devices. The steady state temperature rise corresponds to nearly 100°C for the SOI and 10°C for the bulk devices, respectively. Tenbroek et al. [33] used a small signal conductance technique to estimate self-heating in SOI devices of 2–5 μm length, and found thermal resistances of the order of 2–4 K/mW and thermal time constants of the order of 100 ns. A similar method was used by Jin et al. [34] to explore the width dependence of thermal properties in SOI devices. They have found that for wide ($W > 10$ μm) devices, the thermal resistance scales approximately linearly with $1/W$ (with 60 μm K/mW per device width, i.e., 6 K/mW for a 10 μm wide device), while the thermal time constant is independent of device width because the thermal capacitance and resistance have inverse width dependence. More recently, Jenkins and Polonsky [35,36] have used pulsed *I-V* and off-state leakage luminescence techniques to characterize self-heating in 100 nm gate length SOI transistors, finding thermal resistances of approximately 13 W/mK and thermal time constants between 60–100 ns. Since no new data is available for devices shorter than 100 nm, detailed simulation techniques taking into account the effects of thermal conductivity reduction in ultrathin films (Fig. 8) and of thermal boundary resistance between various materials [21,30] are essential. It is these subcontinuum effects that add up to yield device thermal resistances up to 100 K/mW for the smallest devices of gate lengths near 10 nm, as mentioned in the previous section.

7 Germanium Transistors

Germanium field effect transistors (FETs) were largely abandoned 40 years ago because germanium lacks a reliable, native insulator like SiO_2 for silicon. However, with the recent introduction of compatible high-*k* gate dielectrics, the existence of a viable germanium transistor has become a renewed possibility [37]. Such devices are attractive because germanium has higher low field mobility than silicon (both for electrons and holes), which is thought to determine the ultimate current drive of a device [29]. From a thermal point of view, however, large scale integration with bulk germanium transistors is more problematic because germanium has a thermal conductivity only about 40% that of silicon.

On the other hand, recent calculations suggest that ultrathin film germanium films take on a lesser penalty in their thermal conductivity reduction than thin silicon films, as in Fig. 6. The longer bulk phonon mean free path of silicon also implies a stronger effect of boundary scattering on the thin film thermal conductivity. As the film thickness is reduced, thin germanium films become more attractive (thermally) compared to silicon films vs. the bulk case. The thermal conductivity ratio between the two material films is also plotted in Fig. 6. The bulk thermal conductivity ratio between germanium and silicon is approximately 0.4 (see Table 1), which increases to 0.65 in favor of germanium for the thinnest films of practical interest. On the other hand, germanium devices have a higher mobility, which is less sensitive to temperature compared to silicon [30]. The higher mobility means that between otherwise similar, well-behaved Germanium-on-Insulator (GOI) and Silicon-on-Insulator (SOI) devices, the GOI devices can support the same amount of current (I) at lower operating voltage (V). Moreover, the total dissipated power ($I \cdot V$) is expected to be lower for such GOI devices. Owing to their less temperature-sensitive mobility, and lower power dissipation, well-designed GOI devices are expected to maintain their performance advantage over similar SOI devices, despite the (still) lower thermal conductivity of the thin germanium layer [30]. This thermal behavior makes GOI

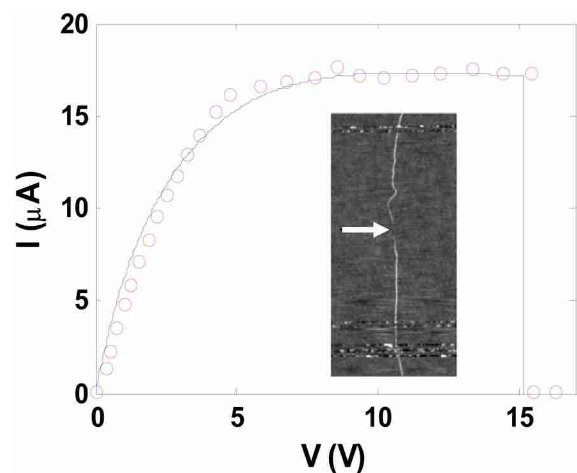

Fig. 9 Current-voltage characteristics of a 3 μm long metallic single-wall carbon nanotube up to breakdown by oxidation (burning) in air, when the middle of the SWNT reaches about 600°C at 15 V bias. The data (symbols) and inset (AFM image showing place of breakdown) are from Ref. [43]. The model (solid line) is described in Ref. [47].

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technology an interesting alternative to SOI for the smallest thin film devices at the limits of the technology roadmap. The lower fabrication temperatures of GOI devices also make them an attractive choice for three-dimensional integrated circuits.

8 Semiconductor Nanowires

Transistors made from semiconductor nanowires (NWs) have recently received a lot of attention for their current-carrying capabilities, low synthesis temperature (as low as 275°C for CVD-grown germanium NWs [38]), and the relative ease of fabrication and integration with currently existing technologies [39,40]. Nanowires also present an ideal vehicle for studying (low-dimensional) electronic and thermal transport at nanometer length scales, as well as coupled electrothermal transport. There are few data available on the mobility and thermal conductivity of nanowires, but it is strongly believed that confined electron and phonon conduction plays an important role in these devices. Recently measured silicon NW thermal conductivity suggests it is on the order of 5 Wm^{-1} K^{-1} for wires of 20 nm diameter [23], which (as expected) is lower than the thermal conductivity of comparably thin silicon films. The theoretical understanding of such transport is still poor, and key simulation tools are not yet available.

Suspended semiconductor nanowires also represent the extreme limit of the electrothermally confined FinFET or trigate (surround-gate) device. Their low thermal conductivity combined with their current-carrying ability imply tight and possibly limiting coupling (especially at high current levels) between electrons and the lattice. In other words, although such devices are known to be adversely affected by poor contact resistance, in practice, their performance may be ultimately limited by self-heating. However, with controlled growth on a large scale, and a solid theoretical understanding from an electrothermal point of view, nanowires could perhaps complement (although not necessarily displace) currently existing CMOS technology.

9 Carbon Nanotubes

Unlike nanowires, carbon nanotubes (CNTs) cannot be synthesized at relatively low temperatures, but rather only in the 550–1100°C range, depending on the method and catalyst used. However, both their electrical and thermal properties are outstanding, such that CNT-based devices may well represent the ultimate limit of nanotransistors. Short CNTs exhibit quantized, ballistic transport at low temperature and low bias, and extremely high current-carrying ability at high bias, up to 100 μA through single-wall tubes of length approximately 15 nm and diameter 2 nm [41]. Until recently, CNT performance was significantly hindered by large contact resistance; however with the introduction of low-resistivity Pd contacts, such devices are one step closer to realizing their potential applications [42]. The existence of good quality contacts has also enabled studies which have shown that for nanotubes much longer than the electron-optical phonon (OP) mean free path (MFP), high-bias electron transport is not truly ballistic [43]. Despite the ballistic nature of CNTs at low-bias (where the intrinsic resistance is close to $h/4e^2 \approx 6.5$ kΩ), strong electron-OP scattering dominates high-field transport, when electrons can attain energies more than 0.16 eV, the zone-boundary optical phonon energy [44].

Recent work has also shown that despite their high thermal conductivity [45], the thermal *conductance* of SWNTs is relatively low, owing to their small diameter [46,47]. The consequences of this low conductance are most evident when high biases are applied across *suspended* SWNTs [46]. Freely suspended, unperturbed SWNTs in vacuum seem to represent the extreme case of a thermally isolated scenario for nanotubes, and for nanoscale devices in general. A key signature of their behavior is the Negative Differential Conductance (NDC) observed at high bias, which is found to be directly dependent on the thermal conductivity behavior $(1/T)$ at high temperatures. SWNTs on insulating substrates have also been recently shown to exhibit self-heating at high-bias, enough to eventually cause breakdown by oxidation (burning) in air at high enough voltage, as shown in Fig. 9 for a 3 μm long tube. This breakdown voltage has been found to scale approximately as 5 V/μm for tubes longer than 1 μm, suggesting a SWNT-to-substrate thermal conductance of about 0.15 WK^{-1} m^{-1} per nanotube length [47]. For much shorter tubes, it appears that high-bias current enhancement is aided by increased heat sinking through the contacts [48] rather than along the length of the tube itself. With these recent advances in understanding electrical *and* thermal transport in SWNTs, the optimization of SWNT transport ought to be possible, consequently yielding more reliable and efficient carbon nanotubes for device and interconnect applications.

10 Concluding Remarks

Traditional heat transfer research for electronic systems has focused on transport off the semiconductor chip, including air convection from the heat sink and conduction in the package. However, semiconductor roadmap (ITRS) trends and the introduction of novel device technologies may eventually cause the temperature rise on the chip, and specifically within nanoscale transistors, to approach or even eventually exceed the temperature rise between the chip and the ambient air. This situation motivates a new era of heat transfer research focused on nanoscale conduction physics, coupled electron and phonon transport modeling, and transistor design optimization. The design of any future nanotechnologies must come with a fundamental understanding of both charge and heat transport at nanometer length scales, and across various materials. The small dimensions affect both current and heat transport via quantum confinement and boundary scattering. The methods and models presented in this review are applicable beyond the silicon-based industry.

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