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Integrated Microchannel Cooling for Three-Dimensional Electronic Circuit Architectures

The semiconductor community is developing three-dimensional circuits that integrate logic, memory, optoelectronic and radio-frequency devices, and microelectromechanical systems. These three-dimensional (3D) circuits pose important challenges for thermal management due to the increasing heat load per unit surface area. This paper theoretically studies 3D circuit cooling by means of an integrated microchannel network. Predictions are based on thermal models solving one-dimensional conservation equations for boiling convection along microchannels, and are consistent with past data obtained from straight channels. The model is combined within a thermal resistance network to predict temperature distributions in logic and memory. The calculations indicate that a layer of integrated microchannel cooling can remove heat densities up to 135 W/cm^2 within a 3D architecture with a maximum circuit temperature of 85°C. The cooling strategy described in this paper will enable 3D circuits to include greater numbers of active levels while exposing external surface area for functional signal transmission.
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Introduction

Three-dimensional (3D) circuit architectures enable the integration of logic with memory, RF devices, optoelectronic devices, and microelectromechanical systems on a single chip. These 3D circuits offer reduced communication delay between modules (e.g., between logic and memory), reduced interconnect length, and even improved reliability [1,2]. However, 3D circuits pose thermal management challenges due to the significant increase in total power generated per unit available surface area for cooling. Furthermore, the power generated per unit volume within a 3D circuit can vary significantly, yielding large junction temperature nonuniformities that can impair the collective operation of the circuit [2]. Another problem is that the increased functionality of the circuit demands greater surface area for input and output of electrical, optical, RF, and other types of signals, which further reduces the surface area available for heat removal. While the semiconductor research community is actively studying the electrical performance and manufacturing methods of 3D circuits with as many as one hundred device layers [3], the introduction of a new cooling approach is a critical issue in its implementation.

The heat removal problem is particularly challenging for vertically integrated circuit (3D IC) technologies [1,2]. The first thermal analysis of 3D ICs addressed concerns regarding heating effects in 3D complementary metal-oxide-semiconductor and investigated the effects of the silicon thickness of the upper chip layers [4]. Previous thermal analysis was performed through device-level [4,5] or chip-level [5,6] modeling, showing that thermal packaging technologies with thermal resistance below 0.5 K/W will be necessary to obtain reasonable chip temperature in 3D ICs. It is also reported that metal thermal vias and Cu bonding layers in 3D integration could be helpful for heat removal in 3D ICs [5]. Figure 1 is a conceptual schematic of a hyperintegrated 3D IC combined with a contemporary flip chip package and heat sink technology. The device layers are vertically separated from each other by interlayer dielectrics, which are very poor thermal conductors with thermal conductivity below 0.3 W/mK for some low-*k* dielectrics [7]. The thermal management challenge can be exacerbated by higher power densities in 3D circuit architectures. While the chip area is reduced, heat generation power per unit surface area will increase. The very large thermal resistance established between the bottom layer and the ambient results in a high junction temperature on the chip.

While there has been much previous research on advanced microprocessor cooling approaches, previous studies have been focused on traditional two-dimensional circuits with a single layer of active circuits. A broad variety of micromachined heat sink technologies include microjet impingement cooling devices [8], capillary loops with microscale evaporators [9], and microchannel heat sinks [10]. Pumped liquid cooling has been implemented in commercial laptop and desktop computers, in many cases exploring novel electrokinetic and electrohydrodynamic pumps [10,11]. These devices have made substantial improvements in the thermal resistance between the chip and the ambient temperature with values approaching as low as 0.1 K/W, and continued research in this field is expected to lead to cooling of 3D circuits as well. However, past work does not address the fundamental thermal management problems faced by designers of 3D circuits, specifically the limited surface area available for cooling and the large vertical thermal resistance between the bottom device layer and the cooling technology.

Figure 2 shows a schematic of the solution strategy proposed in this research, a 3D circuit with multiple layers of integrated microchannels. Heat generated by the device layers can be removed

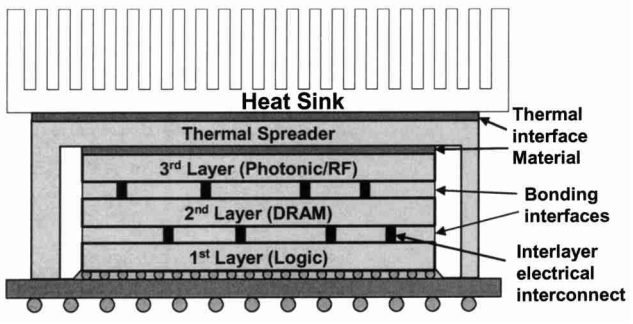

Fig. 1 Three-dimensional circuit architecture connected to a conventional heat removal device

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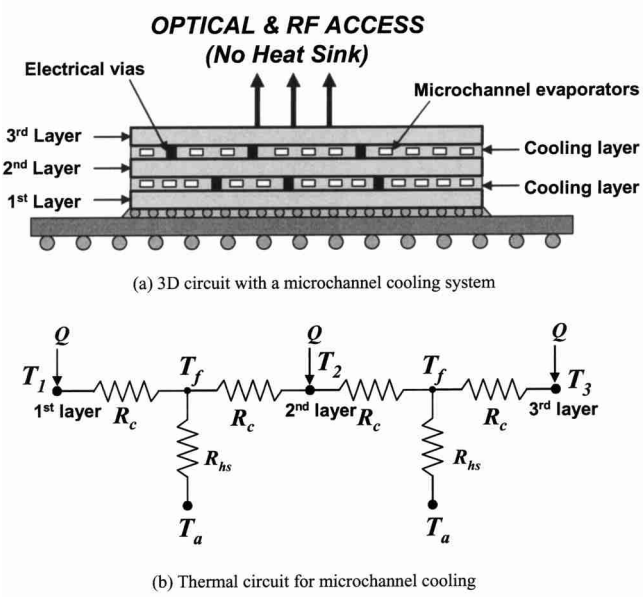

Fig. 2 Conceptual schematic of a microchannel cooling network for a 3D circuit and the thermal circuit model. (*a*) 3D circuit with a microchannel cooling system. (*b*) Thermal circuit for microchannel cooling.

locally to adjacent microchannel layers with low thermal resistance, and the number of device layers can be scaled indefinitely as long as sufficient cooling is provided for each layer. The top surface of the proposed 3D architecture is free and provides electronic and photonic access. Boiling convection cooling in microchannels is particularly promising because of the reduced fluid flow rates required for heat removal and the opportunities it provides for temperature regulation through fluid saturation pressure distribution [10,12]. An integrated microchannel network can achieve a reasonably low thermal resistance while utilizing fluid latent heat and minimizing pumping power. It also has unique attributes of small coolant inventory and fairly uniform temperature profile. Theory and experiments have characterized conduction, convection, and two-phase boiling regimes in microchannels and have shown that they can aggressively cool on-chip hotspots at a reasonable temperature while removing more than 100 W from the chip with a minimal heat sink volume (1 cm$\times$1 cm $\times$1 mm) and chip surface area (1 cm$\times$1 cm) [10,13].

The present work studies theoretically the potential of integrated microchannel cooling networks for removing local high heat generation rates from 3D circuit architectures. A conjugate conduction/convection heat transfer simulation approach solves the steady-state thermal resistance network of device layers and one-dimensional convection equations along the microchannels. It incorporates spatially varying heat transfer coefficients, fluid temperature profiles and pressure drop along the channels, and has been shown to be consistent with previous experimental data for pressure drop and temperature field along straight microchannels. This study examines the effect of hotspot locations on the junction temperature uniformity and the peak temperature. The simulated junction temperature field with the microchannel heat sink is compared with that using a conventional cooling system.

Three-Dimensional Circuit Fabrication Methods

Although this study focuses on the theoretical potential of microchannel cooling for enabling 3D circuits, a much larger challenge will be integrating the process steps for the microfluidic channels within the already demanding process flow required to make 3D circuits. The main goal of 3D circuit processing is creating additional semiconducting layers of silicon, germanium, gallium arsenide, or other materials on top of an existing device layer on a semiconducting substrate. There are several possible fabrication technologies to form these layers. The most promising near-term techniques are wafer bonding [14–17], silicon epitaxial growth [18–20], and recrystallization of polysilicon [21–24]. Figure 3 shows a schematic of 3D circuits illustrating two different fabrication schemes. The choice of a particular technology will depend on the requirements of the integrated circuit system, manufacturability, and process compatibility with current technology. There are a variety of methods available for forming microchannels within a three-dimensional circuit, including plasma

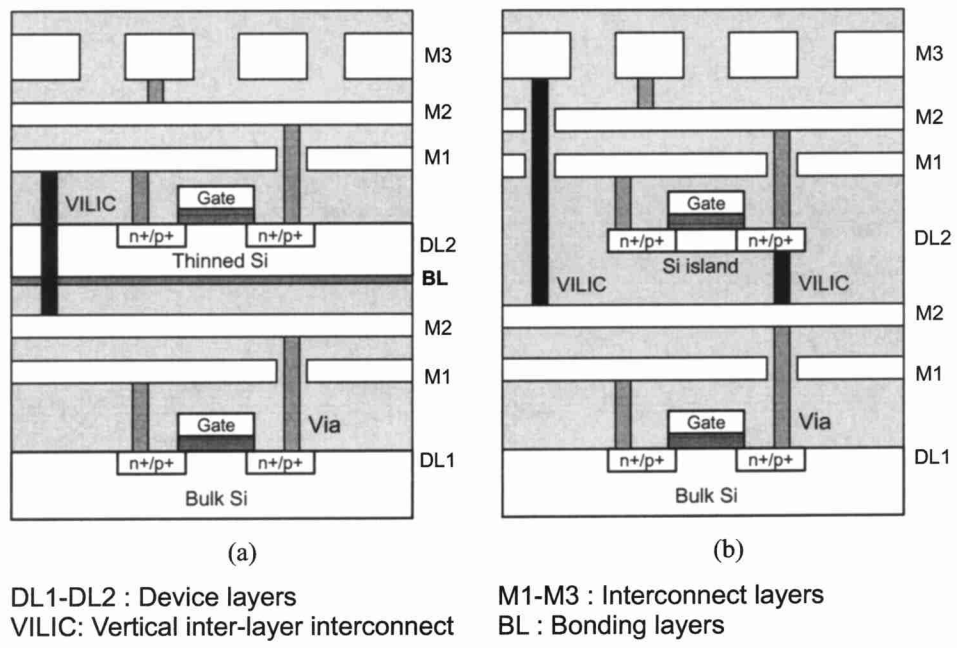

Fig. 3 Schematic of hierarchical 3D circuit structures fabricated by (*a*) wafer bonding, and (*b*) silicon epitaxial growth or recrystallization of polysilicon

etching prior to wafer bonding, sacrificial silicon channels, and even chemical etching. Furthermore, there has been much recent research on etching vertical channels through wafers for electrical connections, which can be leveraged to provide the vertical fluidic connections needed in this research.

Wafer bonding differs from other fabrication technologies due to the opportunity for independent processing of the wafers prior to bonding. Fully processed wafers are directly bonded using various techniques leading to the completely overlapped stacking of the chips. Wafer bonding can be achieved by using polyimide adhesive layers [14], Cu-Cu thermocompression method [15,17] and microbumps with liquid epoxy injection [16]. The wafer bonding process preserves electrical characteristics of each device layer and can be repeated without damaging existing circuits. The alignment tolerance of $\pm 1-2\ \mu$m [1,16] requires careful design of vertical interlayer interconnections.

Silicon epitaxial growth technique utilizes epitaxially grown single-crystal Si islands as device layers. Single-crystal Si islands are formed out of the open seed window by selective epitaxial growth, epitaxial lateral overgrowth, and chemical mechanical polishing of excess Si [18–20]. The major limitation of this technique is high process temperatures ($\sim 1000°$C), which results in significant degradation in the lower device layers especially with metallization layers. Although low-temperature epitaxial Si can be obtained using ultra-high-vacuum systems [25] and utilizing plasma [26], this process is not yet feasible for manufacturing.

Recrystallization of polysilicon [21–24] is another method for forming a second Si layer. This technique deposits polysilicon and induces recrystallization of the polysilicon film using intense laser or electron beams to enhance the performance of the thin-film transistors (TFTs). This technique requires high process temperatures during the melting of polysilicon layers. Beam-recrystallized polysilicon TFTs also exhibit low carrier mobility and unintentional impurity doping. Local crystallization, induced by patterned seeding of Ge [27] or by metal-induced lateral crystallization [28], can enhance TFT performance.

Previous Research on Two-Dimensional Microchannel Heat Sinks

There has been much past research on microchannel cooling in two-dimensional (2D) heat sinks, which forms the groundwork for the modeling study performed in the current study on a 3D microchannel network. Since Tuckerman and Pease [29] demonstrated that single-phase microchannel cooling can remove 790 W/cm^2, much of the subsequent research has focused on the physics and optimization of two-phase flow in microchannels. Perhaps the closest previous work to the current integrated 3D microchannel network is that of Wei and Joshi [30], who proposed stacked microchannels for cooling of microelectronic devices. A number of parallel microchannels are fabricated in the surface of a substrate and then each layer is bonded into a stacked heat sink which is attached to the chip. They proposed a simple thermal resistance network model and performed optimization to minimize the overall thermal resistance.

Past work indicates that the two-phase flow in microchannels exhibits different flow regimes and heat transfer characteristics compared to macroscale convective boiling [31]. Experimental investigation on boiling flow transition in microchannels showed no bubble generation in channels with hydraulic diameters ranging from 150 to 650 μm, although the heat transfer rate suggested that phase change occurred [32,33]. The authors called this phenomenon ''fictitious'' boiling and suggested that it was attributed to the condition $D_h < D_{crit}$, where D_{crit} is the critical diameter at which bubbles are stable considering surface forces and the pressure dependence of the saturation temperature. Bower and Mudawar [34,35] performed a thermal characterization of two-phase microchannel heat sinks with refrigerant as the working fluid and developed a homogeneous model for a two-phase pressure drop simulation. Predictions agreed well with experimental data for heat sinks with channel sizes from 510 μm to 2.54 mm. Stanley et al. [36] performed two-phase flow experiments in rectangular channels using inert gas–liquid water mixtures and proposed friction factor correlations for one-dimensional two-phase flow models. Based on available experimental observations, a gas–liquid two-phase flow regime map was proposed for a near-circular channel whose hydraulic diameter is less than 1 mm [37,38]. Recent experimental observations have shown that two-phase flow regimes in microchannels contain only the slug and annular flow regimes without bubbly flow patterns [13,31,39–45]. Peles et al. [39] proposed a one-dimensional flow model with flat evaporation front dividing the liquid and vapor into two distinct domains based on their experiments with 50 to 200 μm hydraulic diameter channels. Experiments were performed to investigate the flow patterns of two-phase flow in microchannels, to find the temperature distribution along the channels, and to study the effects of convection on chip instabilities [40,41]. They obtained nonuniform temperature distributions, with temperature increasing in single-phase regions and decreasing in two-phase regions. Qu et al. [42–44] performed measurements and predictions of saturated flow boiling heat transfer and pressure drop in a water-cooled copper microchannel heat sink with 21 parallel channels having a 231 μm$\times$713 μm cross section. They examined the conventional correlations for two-phase heat transfer coefficients and proposed a phenomenal annular flow model.

The problem of spatially varying heat flux from the microchannel walls has recently received attention. A homogeneous two-phase flow model has been developed to calculate the fluid pressure drop and junction wall temperature distributions [12,13,46,47]. A closed-loop cooling system was demonstrated utilizing microchannel heat sinks, which were designed using a homogeneous two-phase model [10]. Careful design is important to avoid dry-out and high junction temperatures for stable system operation. It was recommended that the heat sink be attached to the chip such that the hotspot is located near the exit of the channels to reduce the pressure drop along channels and thus leads to a decrease in the peak junction temperature [12,47]. While large thermal resistance of the single-phase region causes a high peak junction temperature, subchannels are incorporated to improve the heat sink performance [47].

Past work on two-phase microchannel cooling was focused on cooling of 2D circuits and on demonstration of a single- or multichannel system ignoring the effects of flow distributions in a channel network. Three-dimensional circuit cooling faces a conjugate heat transfer with 3D thermal conduction and boiling convection in microchannels. In a two-phase microchannel network, each channel experiences flow instability due to the random formation and growth of a void. The instability problem induced by the flow instability is more critical in microchannel cooling of 3D circuits, since more microchannel layers are coupled. These should be addressed to demonstrate an integrated microchannel cooling network for 3D circuits.

Modeling

Figure 4 shows a schematic of the microchannels implemented in a 3D circuit architecture within a coordinate system. It is assumed that the microchannels are distributed uniformly and fluid flows through each channel with the same liquid flow rate. The working fluid, water, flows in the z direction with a mass flow rate of $\dot{m}$. The junction heat generation rate q'' is assumed to vary only in the z direction. Using symmetry, a one-dimensional conjugate conduction/convection heat transfer analysis is applied to only one channel for each layer. The time- and space-averaged one-dimensional energy equations for the jth device layer and channel layer are

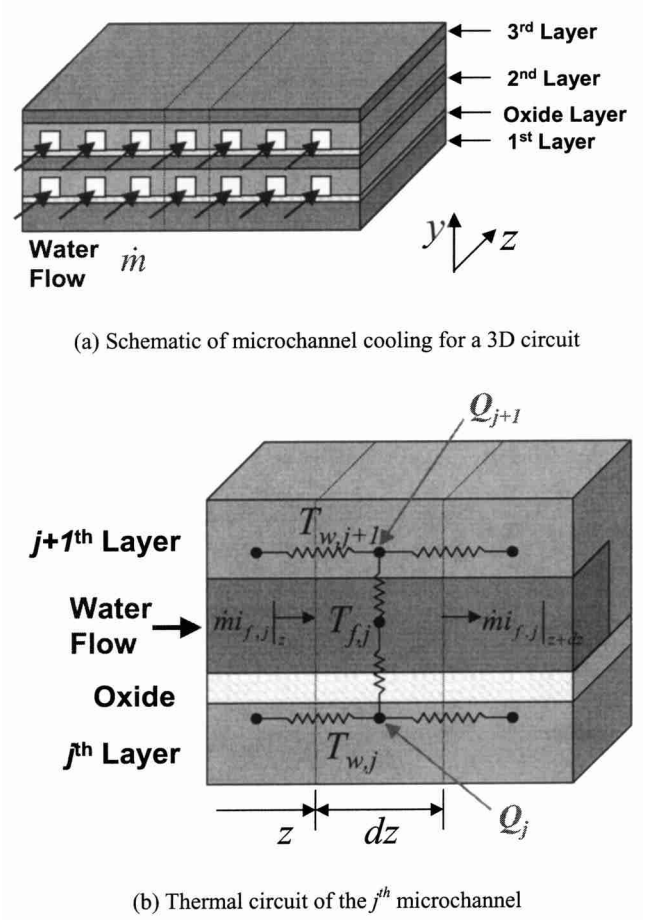

Fig. 4 Schematic of microchannels implemented in a 3D circuit and thermal modeling of microchannel cooling for a 3D circuit. Only one channel is analyzed in a cooling layer by geometric and thermal symmetries. Dotted lines indicate a control volume used in derivation of energy equations [Eqs. (1) and (2)]. (*a*) Schematic of microchannel cooling for a 3D circuit. (*b*) Thermal circuit of the *j*th microchannel.

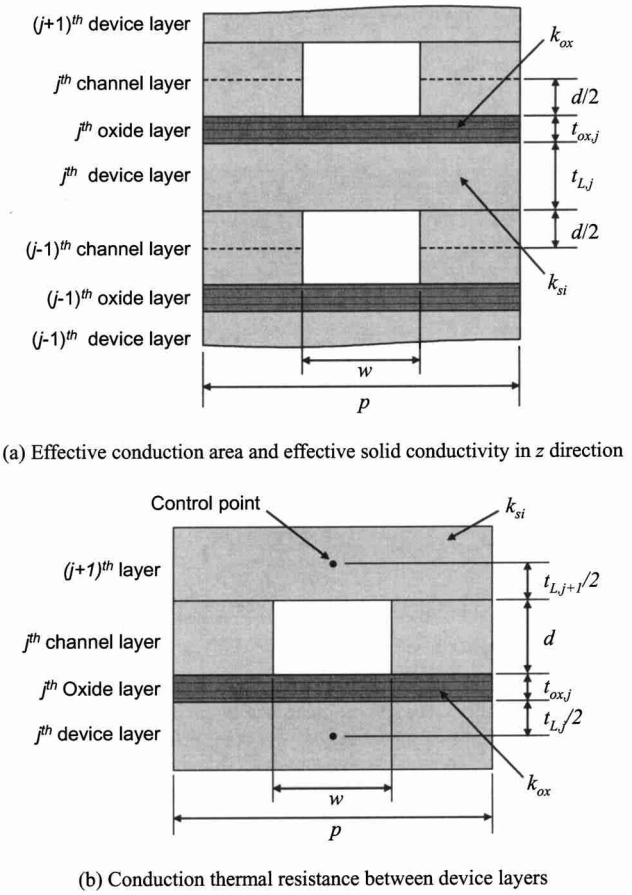

Fig. 5 Predictions for the effective thermal conductance and thermal resistance. (*a*) Effective conduction area and effective solid conductivity in the *z* direction. (*b*) Conduction thermal resistance between device layers.

Solid:

$$\frac{d}{dz}\left(k_{w,z,j}A_{w,j}\frac{dT_{w,j}}{dz}\right)=q''_j p+h_{conv,j}\eta_0(w+d)(T_{w,j}-T_{f,j-1})+h_{conv,j}\eta_0(w+d)(T_{w,j}-T_{f,j})+(T_{w,j}-T_{w,j+1})/R_{th,j}+(T_{w,j}-T_{w,j-1})/R_{th,j-1} \quad (1)$$

Fluid:

$$\dot{m}\frac{di_{f,j}}{dz}=h_{conv,j}\eta_0(w+d)(T_{w,j}-T_{f,j})+h_{conv,j}\eta_0(w+d)(T_{w,j+1}-T_{f,j}) \quad (2)$$

where $T_{w,j}$ and $T_{f,j}$ are the average local temperatures of the solid wall and the fluid, respectively. The subscript j indicates the property of the jth layer. The pitch of microchannels is denoted as p. The depth and width of the microchannel are represented as d and w, respectively. The forced convection coefficient for heat transfer between the solid wall and the working fluid is $h_{conv,j}$. In Eq. (2), diffusion terms are neglected since the Peclet number, defined as $\rho UD_h/\alpha$, is much greater than unity in this study. The fluid enthalpy per unit mass (i_f) is expressed in terms of local thermodynamic equilibrium fluid quality (x) which is the mass fraction of the vapor phase, using

$$i_f=(1-x)i_l+xi_v \quad (3)$$

where subscripts l and v represent liquid and vapor phase in a two-phase flow, respectively. The effective thermal conductivity of solid in the z direction is $k_{w,z,j}$ and $A_{w,j}$ is the effective solid cross-sectional area. From Fig. 5(*a*), effective conduction area in the z direction is obtained as

$$A_{w,1}=(t_{L,1}+t_{ox,1})p+d(p-w)/2, \quad (j=1)$$
$$A_{w,j}=(t_{L,j}+t_{ox,j})p+d(p-w), \quad (j=2\sim jmax-1)$$
$$A_{w,jmax}=(t_{L,jmax}+t_{ox,jmax})p+d(p-w)/2, \quad (j=jmax) \quad (4)$$

where $t_{L,j}$ and $t_{ox,j}$ are thicknesses of the jth layer and the jth oxide layer, respectively, and $jmax$ is the number of device layers. The corresponding effective solid thermal conductivity in the z direction is given as

$$k_{w,1}=\frac{(k_{si}t_{L,1}+k_{ox}t_{ox,1})p+k_{si}d(p-w)/2}{A_{w,1}}, \quad (j=1)$$
$$k_{w,j}=\frac{(k_{si}t_{L,j}+k_{ox}t_{ox,j})p+k_{si}d(p-w)}{A_{w,j}}, \quad (j=2\sim jmax-1)$$
$$k_{w,jmax}=\frac{(k_{si}t_{L,jmax}+k_{ox}t_{ox,jmax})p+k_{si}d(p-w)/2}{A_{w,jmax}}, \quad (j=jmax) \quad (5)$$

where k_{si} and k_{ox} are conductivities of silicon and oxide layers, respectively. In the present analysis, it is assumed that the thermal properties of solid are fixed at constant values. The conduction thermal resistance between control points on layers j and $j+1$, $R_{th,j}$, can be evaluated from Fig. 5(b) and is

$$R_{th,j}=\frac{t_{L,j+1}}{2k_{si}p}+\frac{d}{k_{si}(p-w)}+\frac{t_{ox,j}}{k_{ox}p}+\frac{t_{L,j}}{2k_{si}p} \tag{6}$$

The overall surface efficiency η_0 is employed to simplify the temperature variation in the y direction within the channel walls and is given by

$$\eta_0=1-\frac{d}{d+w}(1-\eta_f) \tag{7}$$

where η_f is the fin efficiency of the fin with insulated tip [48] assuming that the heat transfer coefficient is uniform along the periphery. The solid energy equation [Eq. (1)] accounts for heat conduction along the layer, heat transfer from solid to liquid, and heat transfer to the adjacent layers. The energy balance equation for fluid flow [Eq. (2)] indicates that convection heat transfer from the wall to fluid causes the change of fluid enthalpy. The analysis employs the thermal lumped capacitance assumption in the y direction for each infinitesimal control volume of the circuit layer, and assumes that the bulk silicon temperature is the same as the junction temperature. In the analysis of the two-phase flow, liquid and vapor phases are assumed to be in equilibrium at the fluid saturation temperature and pressure.

One of the important assumptions is that each microchannel has the same liquid flow rate. In multichannel heat sinks, the flow rate of each channel is determined by mass and momentum conservation equations and, in the steady state, requires equal pressure drop along a streamline from inlet to exit manifold for each individual channel [47]. In practical two-phase heat exchangers, the physics of bubble formation and pressure fluctuation can lead to spatial and temporal instabilities in the flow rate. The flow instabilities from one channel can cause oscillations to propagate in the surrounding channels by flow redistribution. This can lead to failure of the cooling system due to control problems and the change of local heat transfer characteristics. The design of inlet and exit manifolds is critical for uniform flow delivery in a 3D microchannel cooling network. One potential solution is for each microchannel layer to have its own manifold and an independent pump, which in turn would increase the design complexity dramatically. A far simpler approach would be to have inlet and exit manifolds for all channels in the network. However, it is difficult to simulate this geometry since there is limited knowledge about vertical fluid delivery coupled in series with a horizontal fluid delivery, in addition to further complications from boiling flow. The present work, however, ignores the variations in flowrate among channels and assumes the same flowrate to each channel in investigating the time- and space-averaged performance of the microchannel cooling for a 3D circuit.

To close the set of governing equations, complimentary relations are required for the convective heat transfer coefficients and the pressure drop. For a single-phase flow region, the heat transfer coefficient, $h_{conv,j}$, accounts for the effect of wall temperature variation in the axial direction [49]. This approach substitutes the fluid temperature in Eqs. (1) and (2) with the inlet fluid temperature, $T_{f,in}$. In evaluating the varying wall temperature effect, the present analysis uses the average temperature and average heat flux of adjacent layers as local wall temperature and local heat flux, respectively. For the two-phase flow, Kandlikar's correlation [50] is employed to calculate the heat transfer coefficient with the assumption of saturated boiling heat transfer and is given as

$$h_{conv}=h_l[C_1Co^{C_2}(25Fr)^{C_5}+C_3Bo^{C_4}F_k] \tag{8}$$

where h_l is the heat transfer coefficient for the liquid phase flowing alone. The factor F_k is a fluid-dependent parameter whose value for water is unity. The first term in the parenthesis accounts for the forced-convection effect on heat transfer and the second term represents the effect of nucleate boiling in regions with low fluid two-phase qualities. In applying this correlation for the present calculations, the forced-convective term is dominant over the nucleate boiling term, while it is assumed that they still capture the essential physics of the boiling process at the microscales. The constants C_1 to C_5 are determined from the value of Co as shown in Table 1. The dimensionless parameters are

Table 1 Constants in Kandlikar's correlation for horizontal channels [50]

Constant	Convective region ($Co<0.65$)	Nucleate boiling region ($Co>0.65$)
C_1	1.1360	0.6683
C_2	−0.9	−0.2
C_3	667.2	1058.0
C_4	0.7	0.7
C_5*	0.3	0.3

*$C_5=0$ with $Fr>0.04$.

$$Co=\left(\frac{1-x}{x}\right)^{0.8}\left(\frac{\rho_v}{\rho_l}\right)^{0.5} \tag{9}$$

$$Bo=\frac{q''}{m''i_{l_v}} \tag{10}$$

$$Fr=\frac{m''^2}{\rho_l^2 g D_h} \tag{11}$$

where ρ_v and ρ_l represent vapor and liquid densities in the saturation state, respectively. The heat of vaporization per unit mass is i_{l_v} and g is the acceleration due to gravity. Kandlikar's correlation was developed for two-phase horizontal or vertical flows in conventional size channels. Even though there is a controversy in applying the conventional two-phase heat transfer correlations to microchannel flows [37,43], some previous studies [10,12,13] supported Kandlikar's correlation in microchannel cooling and this study employs it as a correlation to predict two-phase heat transfer coefficients in microchannels. This correlation was developed for two-phase channel flows with Froude number (Fr) between 1.14 and 19.07. However, Fr of less than 1 is estimated in the present work. Future experimental work will more closely examine the accuracy of this correlation for flows with low Fr values. For simplicity, it is assumed that the two-phase flow is mixed well, and the convective heat transfer is independent of the wall and fluid temperature variations in the axial (z) direction. With these assumptions, the empirical correlation for the two-phase heat transfer coefficient is used without any adjustment from its original form.

For simplicity and efficiency in the calculation, the pressure drop is calculated using a homogeneous model, in which the liquid and gas flow velocities are identical, given by

$$-\left(\frac{dP_j}{dz}\right)=\frac{fm''^2}{2\rho_j D_h}+\frac{d}{dz}\left(\frac{m''^2}{\rho_j}\right) \tag{12}$$

where P_j and m'' represent the pressure and mass flux of fluid flow, respectively. The friction factor for the two-phase flow in a microchannel, f, is proposed by Stanley et al. [36] as

$$f=\frac{97}{Re}, \quad (Re<3000) \tag{13}$$

Equation (13) has been experimentally determined for values of the two-phase Reynolds number relevant for the current work. Although it was developed for the average shear stress along a channel, it is applied locally in the present analysis. The Reynolds number *Re*, evaluated using mean properties of two-phase flow, is written as

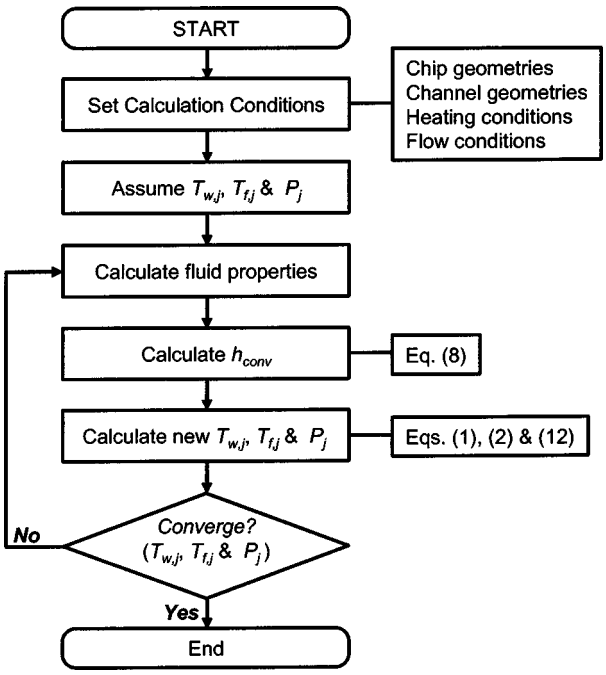

Fig. 6 Flowchart showing the calculation procedure used in this study

$$Re = \frac{\rho U D_h}{\mu} \tag{14}$$

where U is the mean velocity of the flow and D_h is the hydraulic diameter of the channel. For two-phase, the density ρ and dynamic viscosity μ of liquid–vapor mixture are evaluated using

$$\frac{1}{\rho} = \frac{(1-x)}{\rho_l} + \frac{x}{\rho_v} \tag{15}$$

$$\frac{1}{\mu} = \frac{(1-x)}{\mu_l} + \frac{x}{\mu_v} \tag{16}$$

The boundary conditions are adiabatic at both ends of the heat sink for the solid energy equation [Eq. (1)], which ignores conduction loss to the packaging of the microchannel heat sink. For fluid, Eqs. (2) and (12), the inlet fluid temperature and the exit pressure are given to close these equations. The present boundary conditions will overpredict the junction temperatures since they neglect heat loss to the packaging of the microchannel heat sink.

The numerical simulation solves the energy equations for one channel using the finite volume method [51]. Water properties are incorporated using thermodynamic property correlations accounting for their dependence on temperature and pressure [52]. Since this modeling includes strong temperature- and pressure-dependent properties of water, under-relaxation method is employed for convergence. The detailed algorithm is shown in Fig. 6. The number of the nonuniform grid network is 200. The mesh points were densely packed near the inlet. Convergence is declared when maximum relative variations in temperature and pressure between the successive iterations are less than 10^{-5} and when the energy balance has an error of less than 0.1% of the total applied heat. The effects of the grid density are carefully checked to ensure the reliability of the numerical solutions. The model was verified comparing to the experimental data using a 2D microchannel heat sink [10,13]. Good agreements establish confidence in applying this model to microchannels in a 3D circuit. To compare the performances between conventional and microchannel heat sinks, a 3D finite-element simulation is performed using ANSYS to evaluate the thermal performance of a conventional heat sink. For a conventional fin-array heat sink, shown in Fig. 1, the heat sink and thermal spreader are attached to the chip using a conventional thermal interface material. The thermal resistance of a fin heat sink is assumed to be 0.25 K/W and the thermal resistance of the thermal interface material is 0.2 cm^2K/W. The dimensions of a copper heat spreader are 28 mm$\times$28 mm$\times$1 mm. The chip is attached to the center of the spreader. ANSYS calculates the junction temperatures with a constant ambient temperature boundary condition at the top surface of the thermal spreader.

The elevated temperature and pressure may have an impact on the reliability of a 3D circuit. The temperature is, in itself, not an inherent problem in this cooling solution, since the aim of the technology is to reduce both temperature and temperature gradients. However, the high pressures experienced in the channels may induce strain fields in addition to piezoresistive phenomena that can influence the performance of the semiconductor devices. An approximation using beam theory can estimate the effects of pressure on the electrical resistivity of the circuit. The upper wall of the channel is approximated as a beam with fixed ends, with the pressure difference as an applied force. Assuming the pressure difference between the channels in adjacent layers to be 30 kPa, which is close to the maximum pressure gradient of the flow in this study, the maximum stress and strain are about 350 kPa and 3.5×10^{-6}, respectively. The corresponding maximum change in electrical resistance of the circuit is about 0.05%, based on piezoresistive coefficients for bulk silicon. A detailed assessment of this effect is beyond the scope of the present study, which focuses on the heat transfer features of the system. However, it is important to minimize the pressure drop to reduce the effect of temperature and pressure on reliability.

Results and Discussion

Analysis is performed to simulate 3D IC cooling performance with microchannels fabricated between two silicon layers using deep reactive ion etching and wafer bonding techniques [15,17]. Figure 7 illustrates four different 3D stack schemes for a given flow direction. To simulate nonuniform power distributions in practical 3D ICs, the device is divided into logic circuitry and memory, where 90% of the total power is dissipated from the logic and 10% from the memory [53]. This work assumes that the heat generation represents the power dissipation from the junctions and also from interconnect Joule heating. For case (a), the logic circuit occupies the whole device layer 1, while the memory is on the device layer 2. In the other cases, each layer is equally divided into memory and logic circuitry. For case (b), a high heat generation area is located near the inlet of the channels, while it is near the exit of channels for case (c). Case (d) has a combined thermal condition in which layer 1 has high heat flux and layer 2 has low heat dissipation near the inlet. The total circuit area is 4 cm^2, while the total power generation is 150 W.

Table 2 lists the microchannel geometries and simulation conditions. The conventional heat sink/spreader is assumed to be attached on the backside of device layer 1. It should be noted that the microchannel geometry is not optimized since the objective of this study is to identify the characteristics of 3D circuit cooling with microchannels. The channel geometry used in this study is from the past work [12] and gave an optimized performance for 2D chip cooling. The inlet liquid temperature is fixed at 70°C. The saturation temperature of water at atmospheric pressure, 100°C, is too high for very large scale integrated chips whose maximum operating temperature is below 90°C. The fluid absolute exit pressure is fixed at 0.3 bar, which yields a saturation temperature of about 70°C to simulate subatmospheric operation.

Figure 8 compares the thermal performance of the microchannels and conventional heat sinks and plots the predicted junction temperature distributions along the flow direction. In case (a), the heat generation from each layer is uniform and the junction temperature profile with conventional heat sink is symmetric. The microchannel cooling has distinct characteristics of a nonuniform

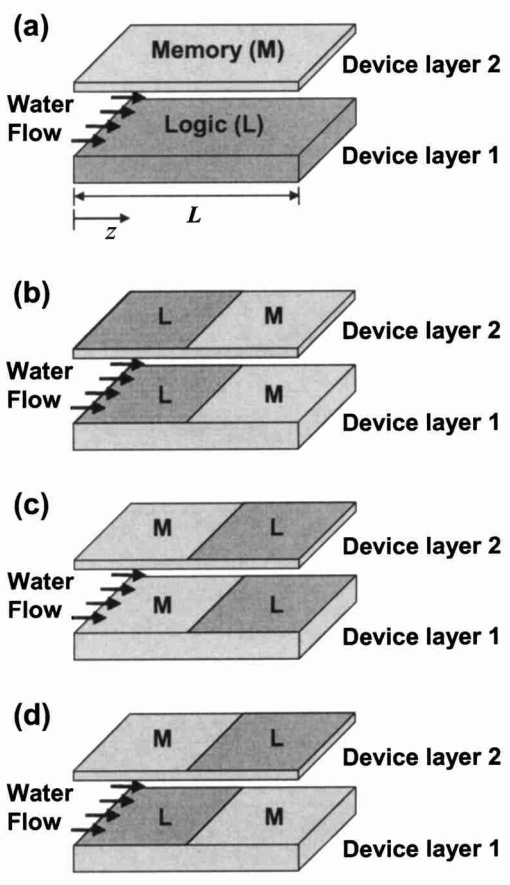

Fig. 7 Two-layer 3D circuit layouts for evaluating the performance of microchannel cooling. The areas occupied by memory and logic are the same and the logic disssipates 90% of the total power consumption [53].

Table 2 Parameters and geometries of a 3D circuit with a microchannel/conventional heat sink

3D circuit architecture	
Chip size	14.14 mm×14.14 mm
Power dissipation	150 W (Logic: 90%, Memory: 10%)
Device layer 1	
Silicon layer thickness	500 μm
Oxide layer thickness	10 μm
Device layer 2	
Silicon layer thickness	20 μm
Oxide layer thickness	10 μm
Microchannels	
Channel layer thickness	400 μm
Number of channels	18
Channel geometry	700 μm (width)×300 μm (depth)
Liquid water flow rate	15 ml/min
Inlet fluid temperature	70°C
Exit fluid pressure	0.3 bar
Conventional fin heat sink with a copper spreader	
Heat sink thermal resistance	0.25 K/W
Thermal interface material	1×10^{-5} m^2 K/W
Copper spreader size	28 mm×28 mm×1 mm

temperature distribution, even under a uniform heating condition. The temperature increases along the channel in the liquid phase region due to sensible heating, and decreases in the two-phase region due to decrease of the fluid saturation pressure along the channel. The junction temperature has its peak at the onsite of boiling point due to the dramatic change in convective heat transfer coefficient from a liquid-phase region to a two-phase region. The temperature difference between layers is greatly reduced by more than 10°C using microchannels because of the small thermal resistance of direct heat removal from layers.

In cases of (b) and (c), identical junction temperature distributions are presented for conventional fin heat sinks. Using microchannels, however, the temperature distribution is quite different, because of the convection nature of flow direction dependence. In both cases, the conventional heat sink presents highly nonuniform junction temperatures of about 25 and 45°C differences for layer 1 and layer 2, respectively, due to the concentrated heat flux. With microchannels, if more heat is applied to the upstream region, boiling occurs earlier resulting in increased pressure drop in the channel. Thus case (c) has a lower pressure drop, lower average junction temperature, and more uniform temperature field than case (b). In case (c), water is gradually heated up in the upstream region, where lower power dissipation is located, and downstream water boils and absorbs heat from the higher power region with low thermal resistance. Since the length of the two-phase region in case (c) is shorter than that in case (b), the overall junction temperature is lower due to a smaller pressure drop. An interesting result for case (c) is that the junction temperature distribution is quite uniform even with highly nonuniform power dissipation, which is one of the powerful merits of the two-phase microchannel cooling.

In case (d), the microchannel heat sink has almost the same pressure drop (26.3 kPa) as in case (a). In both cases, the flow has an identical wall heat rate from the silicon wall to the fluid and the channel fluid temperature profiles are almost identical. The junction temperature is determined by the heat flux and convective thermal resistance from the wall to the fluid. Layer 1 has a high temperature hump near the inlet due to high heat flux and low convective heat transfer coefficient in the single-phase region. The highest temperature in layer 2 is lower than that in layer 1, because of the convective nature of the flow direction dependence and high two-phase convective heat transfer. Except for the temperature hump of layer 1, the overall temperature profile with a microchannel heat sink is more uniform than that using the conventional fin heat sink. In all cases with conventional cooling, the temperature of layer 2 is always higher than that of layer 1 due to larger thermal resistance to the environment.

Concluding Remarks

The present work has theoretically explored the potential of a microchannel network for cooling of 3D circuits. The results indicate that the optimal thermal configuration when using microchannels is to manage the higher power dissipation near the outlet regions since this minimizes the pressure drop of the two-phase flow near the highest heat flux regions and thereby results in a decrease of the local wall temperature. Measurements are needed to confirm this prediction, in particular for the case of a strong spatial variation in the heat flux between regions on the chip. With the peak heat flux of 68 W/cm^2 per active layer, the microchannels keep the predicted maximum junction temperature as low as 85°C. A two-phase microchannel cooling network can achieve a more uniform junction temperature field within a layer and less temperature difference between layers, compared with conventional cooling technology. The maximum junction temperature gradient in a device layer with microchannel cooling in the proposed configuration is as low as 55°C/cm with a maximum junction temperature difference of 13°C, while a conventional cooling system yields 300°C/cm and 45°C. The maximum local tempera-

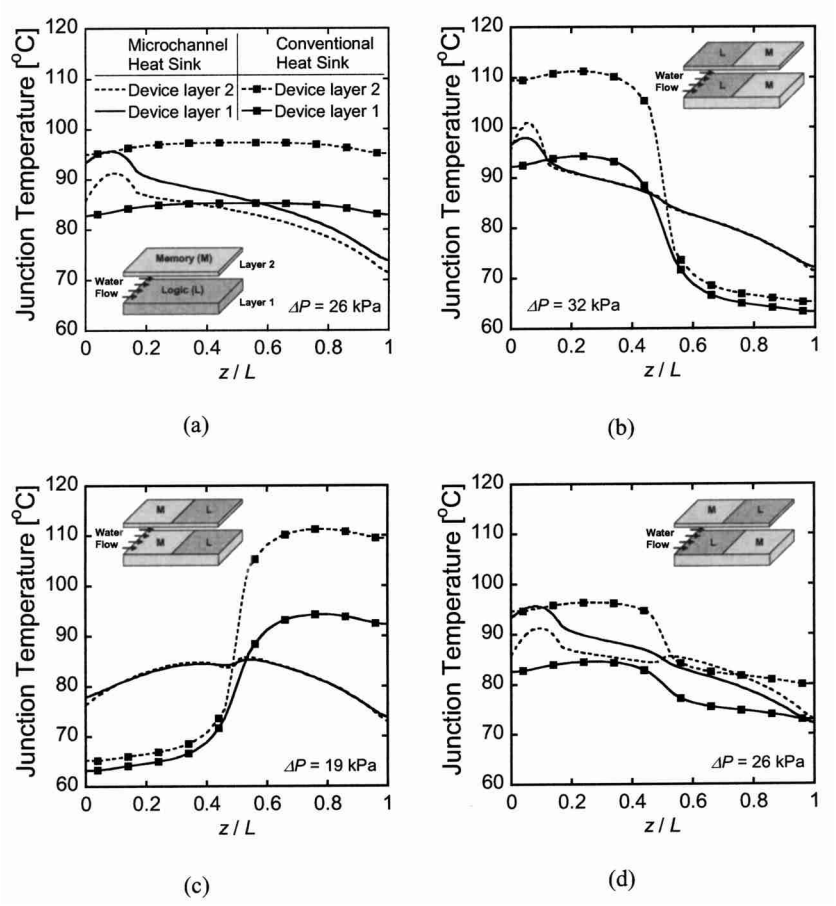

Fig. 8 Comparison of junction temperatures in a two-layer stacked circuit for the cases of an integrated microchannel heat sink and a conventional heat sink. The total flow rate of the liquid water is 15 ml/min and the mass flux is 1.36 $\times 10^{-5}$ kg/s.

ture difference between adjacent device layers is greatly reduced from 15°C by conventional heat sinks to 1.5°C when utilizing microchannels. With two device layers, the liquid flow rate per layer is 7.5 ml/min, and the pumping power, which is the product of pressure drop and the liquid volumetric flow rate at the inlet temperature, is 0.045 W. Generally, when N device layers are involved, the required water flow rate is $15(N-1)/N$ ml/min and the corresponding hydrodynamic pumping power is $0.09(N-1)/N$ W.

Experimental data on boiling convection in 3D microchannel networks are needed to verify the predictions in the current work. Critical is flow delivery to a 3D channel network as well as the potential for severe flow instabilities caused by bubble generation. The design of inlet and exit manifolds is one of the key challenges for the demonstration of a practical 3D circuit cooling system. Further experimental and theoretical work is required to find a relation for two-phase convective heat transfer coefficient. A 3D conjugate conduction/convection simulation is required to calculate the wall temperature under conditions of 3D nonuniform heat generation. Another challenge to be addressed in future work will be the optimization of the microchannel geometries and operating conditions with restriction from the circuit. The present study has illustrated the potential of a 3D microchannel cooling network for removing heat from stacked 3D circuits.

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Nomenclature

A = area, m^2
A_w = solid cross sectional area, m^2
Bo = boiling number
C_1, C_2, C_3, C_4, C_5 = constants in Kandlikar's correlations
Co = convection number
D_h = hydraulic diameter, m
F_k = fluid-dependent parameter in Kandlikar's correlation
Fr = Froude number
L = channel length, m
N = number of device layers
P = pressure, kPa
Q = applied heat, W
R_c = thermal resistance due to convection, mK/W
R_{hs} = thermal resistance due to heat sink system, mK/W
R_{th} = thermal resistance, mK/W
Re = Reynolds number $(=\rho U D_h/\mu)$
T = temperature, °C
U = mean flow velocity, m/s
d = channel depth, m
f = friction factor
g = gravitational constant, m/s^2
h_{conv} = convective heat transfer coefficient, W/m^2K

h_l = heat transfer coefficient for the liquid phase flowing alone, W/m^{2}K
i = enthalpy, J/kg
i_{lv} = latent heat, J/kg
k = thermal conductivity, W/mK
$\dot{m}$ = mass flow rate, kg/s
m'' = mass flux, kg/m^2 s
p = channel pitch, m
q'' = heat flux, W/m^2
t = thickness, m
w = channel width, m
x = thermodynamic equilibrium quality
y, z = coordinates, m

Greek symbols

α = thermal diffusivity, m^2/s
Δ = difference
η_0 = overall surface efficiency
η_f = fin efficiency of the fin with an insulated tip
ρ = fluid density, kg/m^3
μ = dynamic viscosity, kg/sm

Subscripts

L = device layer
a = ambient
f = fluid
hs = heat sink system
in = inlet
j = layer index
$jmax$ = number of device layers
l = liquid
ox = oxide layer
si = silicon
v = vapor
w = silicon wall

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