Managing heat for electronics

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Increasing power densities and decreasing transistor dimensions are hallmarks of modern computer chips. Both trends are increasing the thermal management challenge within the chip and surrounding packaging, as well as accelerating research progress on high-conductivity materials. This article reviews recent materials advances with a focus on novel composite substrates and interface materials, including those composites leveraging the high conductivities of carbon nanotubes. Furthermore, attention is given to the special properties of one-dimensional structures that are likely to be of increasing importance in future applications.

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Thermal management is widely recognized to be an important aspect of computer design, with device performance being significantly affected by temperature. In addition, device lifetime can be decreased drastically because of large thermal stresses that occur especially at interfaces. The ability of a structure to remove heat is best quantified by its thermal resistance, which is given by the temperature difference divided by input power. In microprocessor design, the allowable temperature drop between the transistor (where most of the heat is generated) and the ambient air is constant. As a result, the challenge for thermal management is to develop high-conductivity structures that can accommodate this fixed temperature drop with the increasing power densities that characterize new generations of microprocessors.

Fig. 1 shows the key components that contribute to the thermal resistance of a microprocessor device. First, heat must traverse the chip and heat spreader, where a portion of the allowable temperature drop occurs. Second, the heat sink conducts heat away from the active regions.

Three driving forces are placing stringent demands on materials for thermal management. First, the drive to improve speed motivates circuit designers to compress the 'core' of the microprocessor, which contains the region of the most electrical activity, to ever smaller sizes. This gives higher rates of heat generation per unit area. As a result, the temperature drop caused by solid conduction within the chip

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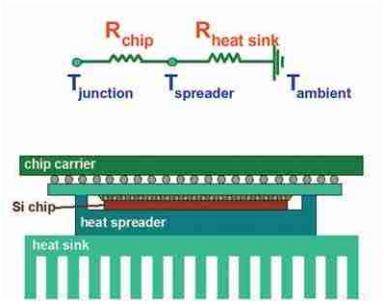

Fig. 1 Schematic of a Si microprocessor, heat spreader (typically made of Cu), and heat sink mounted on a chip carrier. Conventional thermal resistance components include conduction in the chip, and conduction and convection within the heat sink.

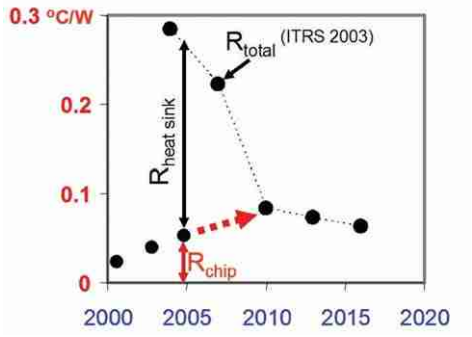

Fig. 2 Thermal resistance components in the design of contemporary and projected high-performance electronic systems, according to the 2003 International Technology Roadmap for Semiconductors[1]. The required total thermal resistance is decreasing because of increasing power densities and a constant allowed temperature drop. However, chip and spreader thermal resistance is predicted to increase to the point where it is comparable to the total allowed resistance. As a result, there is no room for a temperature drop or resistance at the heat sink.

and heat spreader is predicted to become comparable to the maximum allowed temperature drop. The situation is shown by trends mapped out in Fig. 2[1], where the thermal resistance of the chip is predicted to be comparable to the total allowable resistance by 2010. The problem is compounded by exploratory three-dimensional circuits, which increase connectivity but also increase the difficulties associated with heat removal[2]. Second, the temperature rise in interconnects between transistors is growing, owing to increases in the number of metal layers and increasing interconnect current densities and aspect ratios. The problem is made worse by the planned transition to interconnect passivation with lower dielectric constants than SiO_2. Finally, there is the increasing temperature rise within contemporary and planned transistor technologies[1]. Decreasing channel dimensions increases the power density and electron-phonon nonequilibrium within devices, and novel device geometries (e.g. silicon-on-insulator, nanopillars, and fin-shaped field-effect transistors) offer greater thermal resistances to the bulk substrate.

These trends pose important challenges and opportunities for fundamental research in materials and solid-state physics. Heat conduction occurs via the motion of electrons and phonons. While the bulk properties of the materials determine the fundamental transport and scattering of these heat carriers, the properties of interfaces and finite dimensionality are key issues in applications.

This review examines challenges and issues related to thermal transport in materials and structures for electronic applications. In the next section, we describe issues related to composite substrates and heat spreader technologies. In the third section, one-dimensional transport in nanowires and nanotubes is explored. In the fourth section, the role of nanotubes in thermal interface materials (TIMs) is examined. While much of the review describes experimental work, theoretical approaches and results will also be presented.

Heat spreaders and composite substrates

Heat spreaders represent the closest possible location of high thermal conductivity materials to the microprocessor heat source. This allows them to spread heat, as well as reduce peak and average heat fluxes and associated temperature drops, for the largest possible fraction of the resistances in the system. By a large margin, the most common spreader material is Cu. More expensive, commercially available alternatives include vapor chambers, which are two-dimensional, capillary-driven fluid convection devices, as well as diamond, SiC, and AlN substrates. Diamond is clearly the optimal material of choice and has been available synthetically for decades. However, cost has limited this material to all but niche applications, including expensive laser diodes. Diamond coating of spreaders represents a cheaper alternative. Even more expensive spreaders can be made from composites of materials with varying thermal, electrical, and mechanical properties. Examples include Cu-Mo spreaders with thermal expansion coefficients matched to the microprocessor substrate, and diamond/AlN/Mo substrates, which provide improved combinations of heat conductivity, overall heat capacity, and electrical permittivity for radio-frequency devices[2].

The most challenging heat-spreading research, from a materials viewpoint, involves the direct combination of high thermal conductivity materials within the microprocessor substrate. Composite substrates can reduce the substrate's thermal resistance for conduction while spreading the heat laterally, thereby reducing the temperature rise within the

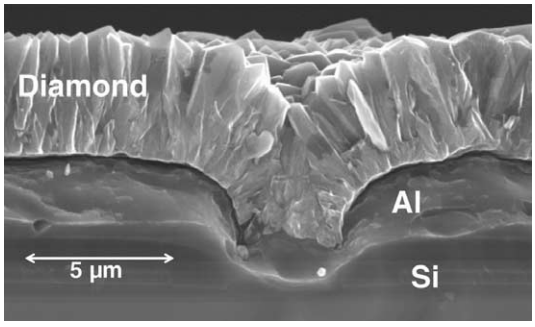

Fig. 3 Diamond deposited on Al in a Si substrate using a microwave plasma technique. (Courtesy of DaimlerChrysler, materials research group.)

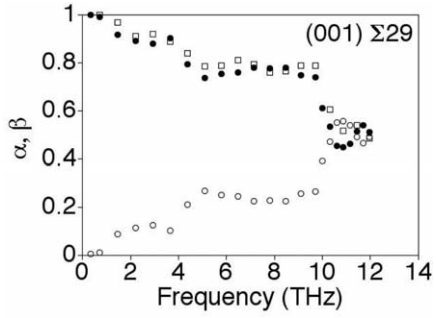

Fig. 4 Energy-transmission coefficients α (filled circles) and reflection coefficients β (open circles) for longitudinal acoustic phonons incident on a Σ29 grain boundary in Si. For long wavelengths and low frequencies, most of the incident energy is transmitted through the boundary. Only for high frequencies does the interfacial scattering become diffuse. The open squares are data for a system with larger transverse dimensions. (Reprinted with permission from[9]. © 2004 American Institute of Physics.)

interface materials and heat sink. To have an impact, the high-conductivity region must be located very near the heat source, i.e. within a distance comparable to the lateral extent of the source. The use of metallic regions embedded within a substrate has been demonstrated for more than a decade in the case of GaAs circuits, specifically through the integration of Au trenches deep within the substrate. This costly deposition process is warranted in high-power transistors and semiconductor lasers, where heat removal can have a direct impact on performance. An alternative to composite substrates is the direct deposition of high-conductivity materials as part of, or above, the metallization layers, which facilitates spreading of heat away from the warmest transistors and interconnects. Fig. 3 shows an example of diamond deposited directly on Al in this configuration. The benefits of diamond in this geometry are severely limited by the high resistances of oxide passivation lower in the multilevel stack, unless this can be eliminated.

For Si circuits, in which the substrate is already a very good heat conductor (~130 W/mK at room temperature), diamond is the only truly promising option for a second material in a composite substrate[3]. Deposition of diamond on Si has been a reasonably mature technology for more than a decade[4], and there are now multiple techniques that provide high-quality polycrystalline films with growth rates exceeding several micrometers per hour. Fabrication methods include direct growth of diamond on the backside of a Si substrate, bonding of a polished diamond film onto a Si wafer, and deposition and thermal recrystallization of polysilicon on top of a diamond film. In each of these cases, the primary challenge is minimization of the thermal resistance between the active Si regions and the diamond. For the case of diamond deposition on Si, the thermal resistances are caused by small grains and phase or stoichiometric impurities in the diamond near the interface. The effective resistances from these imperfections can approach 10^{-7} m^2K/W, which is comparable with an additional 10 μm of Si. Measurement of thermal resistance at the diamond-Si interface has been pursued using optical and electrical methods[5] that are not in widespread practice at present, so it is unlikely that industry will quickly address the problem of interface resistance.

It is clear from the preceding paragraphs that an understanding of the thermal resistance of interfaces is key to identifying limits on heat-removal technologies. From a theoretical point of view, the key issue is to determine how the carriers of heat (electrons and phonons) are scattered at interfaces. Theoretical calculations of phonon conduction across interfaces have largely relied on the diffuse-mismatch model (DMM), which regards interfaces as completely efficient at scattering phonons[6,7]. However, results of this approach are often at odds with experiment. Recently, Majumdar and Reddy[8] showed that accounting for electron-phonon scattering adds an additional resistance that helps to bring theoretical predictions and experiment into better agreement in the case of a metal-insulator interface. On the other hand, recent molecular dynamics simulations of grain-boundary phonon scattering in Si have shown that the DMM represents a limiting case rather than a general rule (Fig. 4)[9]. In summary, it is apparent that, while the DMM is a good first approximation for interfacial scattering, there is plenty of room for refinement of theoretical predictions.

Thermal transport in one dimension: nanotubes and nanowires

Nanotubes and nanowires are one-dimensional structures with diameters ranging from 1 nm to several hundred

nanometers, and lengths from 100 nm to hundreds of microns. Carbon nanotubes (CNTs) were the first to be discovered[10]. A single-walled CNT, or SWNT, can be thought of as a single graphene sheet that is wrapped into a cylinder with a diameter of about 1 nm, while a multiwalled CNT (MWNT) consists of concentric graphene cylinders with a diameter of the order of 10 nm. SWNTs can be either metallic or semiconducting, depending on the diameter and chiral angle, while MWNTs are metallic. CNTs have found applications as field-effect transistors (FETs)[11] and in field-emission displays. Following the discovery of CNTs, a variety of nanowires with filled cross sections has been synthesized. These include nanowires of Si, Ge, GaAs and other III-V materials, Bi and its alloys, and metal oxides such as SnO_2 and ZnO. These nanowires exhibit unique properties and are being explored to fabricate solid-state lasers, optical waveguides, ultrasensitive chemical and biomolecular sensors, high-Q mechanical resonators, and thermoelectric devices.

Nanotubes and nanowires have unique thermal and thermoelectric properties that give rise to new opportunities in thermal management of electronic devices. Theoretical calculations indicate that the room-temperature thermal conductivity κ (the heat current density divided by the temperature gradient) of SWNTs is as high as 6000 W/mK, i.e. higher than diamond or graphite[12-14]. In contrast, it is thought that the κ values of nanowires can be much lower than bulk materials because surface roughness scatters phonons. It has also been suggested[15] that phonon dispersion in nanowires can be different from the bulk because of confinement in the radial direction, lowering phonon group velocity and κ. Suppressed κ values can be used to advantage in minimizing conduction heat loss in thermoelectric coolers and generators[16]. With potential further improvements in the thermoelectric power factor arising from the confinement of electrons, theoretical calculations suggest that a high thermoelectric figure of merit could potentially be obtained in Bi-based[17] and III-V[18] nanowires.

The thermal properties and promising applications of CNTs have stimulated intense experimental investigation. For a randomly aligned mat of nanotube ropes, Hone *et al.*[19] observed a room-temperature κ value of 35 W/mK. The low value is attributed to the presence of a large density of interfaces and voids. A significantly improved κ value of >200 W/mK was measured for dense, thick films of aligned SWNTs produced by filtration/deposition from suspension in strong magnetic films[20]. For isolated nanotubes, experimental measurements come much closer to theoretical predictions. Kim *et al.*[21] have measured $\kappa(T)$ for individual MWNTs using a microfabricated sensor device[22]. The room-temperature κ value exceeded 3000 W/mK (Fig. 5). Preliminary results indicate that κ values of individual SWNTs can be comparable to, or even higher, than individual MWNTs[23].

The observation of high κ in CNTs has led to efforts to develop thin films of CNTs and carbon nanofibers as new TIMs. These could replace thermal grease or phase-change materials (PCMs) for enhancing contact thermal conductance in electronic-packaging applications. The results for CNT-Cu composites[24] and CNT-PCM composites[25] appear to be encouraging in reducing interfacial resistance. To realize κ values that approach those for isolated CNTs, new techniques are needed to reduce interfacial resistance between CNTs and the contacting surface, and between interconnected CNTs in a film. In particular, the resistance between the nanotube or nanofiber and the contacting surface needs to be examined carefully. Yu *et al.*[26] have used a microfabricated device to measure thermal conductivity and contact thermal resistance between a planar surface and an individual carbon nanofiber grown using plasma-enhanced chemical vapor deposition (PECVD). The thermal conductivity of the carbon nanofibers was ~14 W/mK, comparable to that of graphite fibers grown by pyrolysis of natural gas prior to high-temperature heat treatment. To use these PECVD-grown nanotubes and nanofibers as TIMs, therefore, it is necessary to anneal the carbon nanofiber film at high temperatures to reduce defect density and improve the intrinsic thermal conductivity. Yu *et al.*[26] have also measured the contact thermal resistance between the nanofiber and supporting substrate. They found

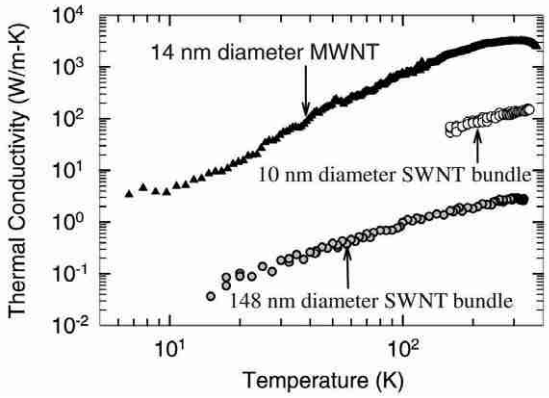

Fig. 5 Measured thermal conductivities of an individual 14 nm diameter MWNT (from[21]), a 10 nm diameter SWNT bundle, and a 148 nm diameter SWNT bundle (from[22]).

that heat-conduction models based on Fourier's law can underestimate the contact resistance at the nanoscale constriction unless the large (25 times) reduction in the thermal conductivity of the constriction is taken into account. The large contact thermal resistance between the CNT and the surface can be a problem. Hu *et al.*[27] noted that the contact thermal resistance between a vertically aligned CNT film and a planar heater surface is large (even with increased contact pressure) compared with the resistance of the CNT film itself. One problem is that not all of the CNTs in the film contact the opposing surface because the CNTs are not uniform in height. A more detailed discussion on TIMs containing CNTs is given in the next section.

The microdevice has also been used to measure $\kappa(T)$ of nanowires[28]. The κ values of Si nanowires and SnO_2 nanobelts decrease with decreasing diameter or thickness. Calculations based on a full-dispersion transmission function approach suggest that increased phonon-boundary scattering is the dominant effect, leading to suppressed κ values for Si nanowires larger than 37 nm in diameter[29] and SnO_2 nanobelts thicker than 50 nm[30]. For a 22 nm diameter Si nanowire, additional phonon confinement effects may play a role. Molecular dynamics simulations have been used to probe the regime of very small sizes[31]. Wave-packet dynamics simulations are being used to study scattering in Si nanowires with the goal of understanding the detailed microscopic scattering mechanisms[32]. In Fig. 6, we show the energy transmission coefficient through a simple interface created by a mass discontinuity. The surprising structure of the result suggests that frequency- and size-dependent scattering may be important in understanding thermal transport in nanowires for very small nanowires (<30 nm).

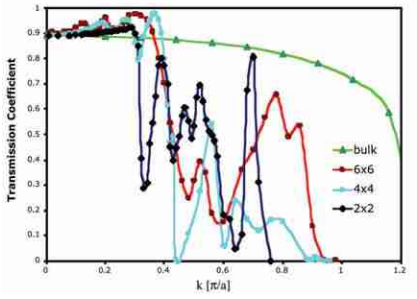

Fig. 6 Energy transmission coefficients for longitudinal acoustic waves incident on a simple interface in a Si nanowire as a function of wave frequency. The interface is a mass discontinuity, with the atoms in perfect registry across the interface. The results for nanowires with cross sections of 2 x 2, 4 x 4, and 6 x 6 unit cells, ranging in diameter from 1 nm to 3 nm, are strongly size dependent, but not in an obviously regular way. Results for a bulk system are included for comparison. (Reprinted with permission from[32]. © 2004 Wiley.)

Thermal interface materials containing carbon nanotubes

The past decade has brought significant developments in TIMs for electronic systems. These materials are typically found between the microprocessor chip and heat spreader (Fig. 1), as well as between the heat spreader and heat sink. Interface materials are subject to challenging requirements, including the ability to reduce thermal stress between regions with vastly differing thermal expansion coefficients, the ability to be reworked, low viscosity at application temperatures, and high thermal conductivity[33]. Common TIMs include a variety of polymer-based materials with high thermal conductivity particle inclusions, typically with diameters of 2-25 μm. The effective thermal conductivities of particle-filled polymer interface materials are typically about an order of magnitude higher than the polymer matrix alone, i.e. of the order of 2 W/mK. The resistance found in commercial products can be substantially larger than anticipated values owing to resistances at the TIM boundaries and small voids, and the total resistance can be significant compared with the limiting values in Fig. 2. This has motivated recent progress on using solders, which provide conductivities in the range of 10-100 W/mK, but these metallic TIMs are less attractive owing to their mechanical stiffness.

Recent research has focused on nanoparticle inclusions, in particular bundles of CNTs, for improving the thermal conductivity of interface materials. Soft materials with CNT inclusions promise near-ideal thermal and mechanical properties. CNTs offer very high thermal conductivities exceeding 1000 W/mK based on cross-sectional area. These values are comparable with the highest-performance filler dielectric materials used in TIMs at present. Furthermore, CNTs offer directional thermal conductivity along with flexible geometry. This unique combination provides an opportunity for combining low effective values of resistance and elastic modulus. An innovative example uses oriented CNTs grown vertically from one surface and forced into contact with the opposing surface[34]. This approach has the potential to yield high effective conductivity in the required direction of propagation, while remaining mechanically flexible in the orthogonal direction, as required for reducing thermal stress. However, there remain many challenges in achieving low thermal resistance between the CNT and the interface opposing the growth surface.

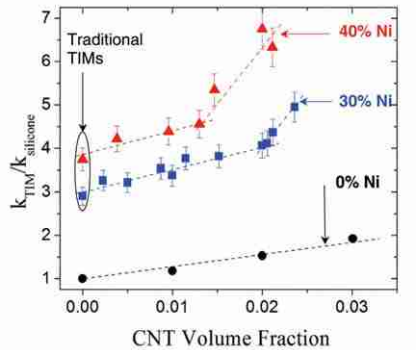

Fig. 7 Thermal conductivity of silicone-based TIMs with varying volume concentrations of Ni particles and MWNTs. The effects of the two filler media become interactive beyond ~0.02 volume fraction of CNTs.

A less challenging use of CNTs in interface materials is as filler particles in a standard soft matrix. Fig. 7 shows experimental data for thermal conductivities of silicone-based interface materials containing varying concentrations of nanotubes and Ni particles[27]. The relative increase in the effective conductivity is less than a factor of two for small volume concentrations of nanotubes below 0.03, and the absolute value remains well below the conductivities of the conventional particle-filled interface material. Beyond these modest volume concentrations of nanotubes, informal data suggest that the rheological and mechanical properties of CNT-filled interface materials become unacceptable for applications. A promising effect has been observed for CNT volume fractions above ~0.02 when the two types of particles are combined. As Fig. 7 shows, the relative impact of an increase in CNT volume fraction is amplified by the presence of conventional particles. This transition is consistent with a percolation model including thermal interconnections formed by CNTs between particles.

In summary, the use of CNTs in interface materials is promising because of the unique combination of rheological and thermal properties. However, more work is needed to realize this potential, particularly in achieving thermal contact between surrounding surfaces and the nanotubes.

Conclusions and outlook

The important issues and current technologies of high thermal conductivity materials for electronics applications have been explored. A recurrent theme is the importance of understanding and limiting interfacial thermal resistance. In order to realize the promise of high thermal conductivity materials like diamond and CNTs, experimental approaches must be found to characterize and control interfacial properties. Theoretical methods, including molecular dynamics simulations, are also expected to play a vital role in elucidating the fundamental limitations of ideal interfaces. MT

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