Phonon-boundary scattering in thin silicon layers

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Temperature fields in microdevices made from silicon-on-insulator (SOI) wafers are strongly influenced by the lateral thermal conductivity of the silicon overlayer, which is diminished by phonon scattering on the layer boundaries. This study measures the thermal conductivity of single-crystal silicon layers in SOI substrates at temperatures between 20 and 320 K using Joule heating and electrical-resistance thermometry in microfabricated structures. Data for layers of thickness between 0.4 and 1.6 μm demonstrate the large reduction resulting from phonon-boundary scattering, particularly at low temperatures, and are consistent with predictions based on the phonon Boltzmann transport equation. © *1997 American Institute of Physics.* [S0003-6951(97)02739-3]

Thin single-crystal silicon layers are becoming more common in microfabricated sensors, actuators, and transistors. These microdevices can be fabricated from silicon-on-insulator (SOI) substrates, which provide silicon layers of thickness between 0.05 and 10 μm above a buried silicon dioxide layer. The performance and reliability of microdevices made from SOI substrates can be strongly influenced by lateral thermal conduction in the silicon layer. This is particularly important for transistors in SOI circuitry,[1] in which thermal conduction in the silicon device layer strongly reduces the peak temperature rise.[2] Microcantilevers made from SOI substrates are promising for high-density thermomechanical data storage[3,4] and have thermal response times and sensitivities governed by thermal conduction along the silicon layer. The thermal conductivity of silicon layers of submicrometer thickness may be strongly reduced by interfacial effects, although this has not been demonstrated previously.

The thermal conductivity of silicon is dominated by phonon transport and, for the case of thin films, can be reduced by phonon scattering on boundaries and by imperfections related to the fabrication process. While phonon-boundary scattering is most important at low temperatures, where the mean free paths of phonons are longest, boundary scattering may also be very significant at room temperature and above in very thin silicon layers.[5] There are no data available to conclusively demonstrate this phenomenon in silicon layers of submicrometer thickness. Previous work[6–8] measured the lateral thermal conductivity of thin polysilicon layers in microsensors and reported a thermal conductivity reduction of up to 80% compared to that in bulk silicon. However, phonon scattering on grain boundaries is responsible for a large fraction of the thermal conductivity reduction in these layers, such that these data are inappropriate for the single-crystal layers in SOI substrates.

This letter provides data and phonon transport analysis that quantify the impact of phonon-boundary scattering on heat conduction in crystalline silicon layers. The data are useful for thermal modeling of microdevices made from SOI substrates. Furthermore, since the purity and microstructural quality of silicon layers in SOI wafers are not far inferior to those of bulk silicon, the conductivity reduction in thin layers provides information about other phonon scattering mechanisms in bulk silicon.

The experimental data are obtained using the microfabricated structure shown in Fig. 1 using a procedure that is detailed in a full-length manuscript.[9] Heat is generated by a steady-state electrical current sustained in a heavily doped region in the silicon overlayer, resulting in a temperature distribution in the silicon that decreases exponentially with increasing x. The temperature distribution in the silicon is detected using electrical-resistance thermometry in two patterned aluminum bridges. The aluminum bridges carry very small current densities and experience negligible Joule heating, such that they measure the silicon temperature in regions surrounding $x=x_A$ and $x=x_B$, respectively. The exact solution is well approximated by

$$T(x)-T_0=\frac{P'}{2}\sqrt{\frac{d_0}{k_0 d_s k_s}}\exp\left(-\frac{x-x_0}{L_H}\right), \tag{1}$$

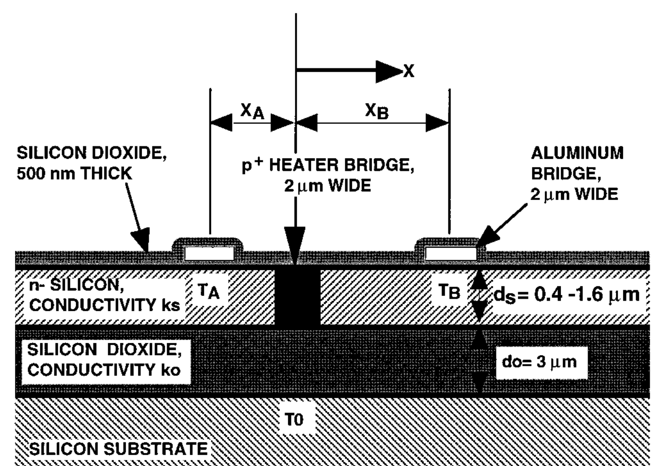

FIG. 1. Cross-sectional schematic of the experimental structure used to measure the lateral thermal conductivity of single-crystal silicon layers in SOI substrates. To achieve a small uncertainty, the separations x_A and x_B need to be somewhat less than the thermal healing length in the device, $L_H=(d_s d_0 k_s/k_0)^{1/2}$. The present study uses $x_A=5$ and $x_B=10$ μm.

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where P' is the heater power per unit length, T_0 is the substrate temperature beneath the structure, d_s and d_o are the silicon and oxide thicknesses, respectively, k_o is the vertical thermal conductivity of the oxide, and k_s is the lateral thermal conductivity of the silicon. The length $x_0 = 0.4 - 0.6\ \mu$m is obtained for each measurement point by matching the temperature distribution from Eq. (1) to the solution of the one dimensional heat conduction equation that includes the 2-μm-wide heated region in the calculation domain. The thermal healing length along the device layer, $L_H = (d_s d_o k_s / k_o)^{1/2}$, is the characteristic length scale of the temperature decay to T_0. For each measurement, the oxide thermal conductivity k_o is measured on the same die using Joule heating and electrical-resistance thermometry,[10] allowing T_0 and k_s to be determined from the measured temperature rises at $x = x_A$ and $x = x_B$ and Eq. (1). The sample is bonded and packaged and cooled using a liquid-helium refrigeration system.[9] The wafers in the current study are fabricated using BESOI technology,[11] which achieves the silicon overlayer through bonding of two thermally oxidized substrates and a subsequent etch. Data reported here were measured on wafers with silicon device layer thicknesses of $d_s = 0.42$, 0.83, and 1.6 μm and buried oxide thickness $d_o = 3\ \mu$m.

The analysis uses a version of the thermal conductivity integral for silicon,[12] which accounts for phonon dispersion and distinguishes between the contributions of transverse and longitudinal modes, together with a solution to the Boltzmann transport equation along thin layers.[13] The modified form of the conductivity integral is

$$k = \sum_{i=L,T1,T2} \frac{1}{3} \nu_i^2 \int_0^{\Theta_i/T} C_i(\tau_b)_i F\left(\frac{d_s}{(\Lambda_b)_i}\right) dx_\omega, \qquad (2)$$

where the subscripts $i = L$, $T1$, $T2$ refer to the single longitudinal and the two transverse phonon modes, respectively, ν_i is the appropriate phonon group velocity, Θ_i is the Debye temperature of the solid, $x_\omega = h_p \omega / k_B T$ is the nondimensional phonon frequency, C_i is phonon specific heat per unit volume and nondimensional frequency, the Boltzmann constant is $k_B = 1.38 \times 10^{-23}$ J K^{-1}, and Planck's constant divided by 2π is $h_P = 1.602 \times 10^{-34}$ J s. The conductivity reduction due to phonon-boundary scattering is calculated independently for each differential step in the phonon frequency spectrum using the solution to the Boltzmann equation, which is realized through the function F. The relaxation time in the absence of phonon-boundary scattering, τ_b, is that determined previously for bulk silicon.[12] The boundary scattering reduction function F depends on the ratio of the layer thickness, d_s, and the appropriate phonon mean free paths for transverse and longitudinal modes, $(\Lambda_b)_i = \nu_i\ (\tau_b)_i$. The reduction function F is calculated using the exact solution to the Boltzmann equation for the mean-free path reduction along a thin layer[13]

$$F(\delta) = 1 - \frac{3}{8\delta^2} + \frac{3}{2\delta^2} \int_1^\infty \left(\frac{1}{t^3} - \frac{1}{t^5}\right) \exp(-\delta t)\, dt, \qquad (3)$$

where $\delta = d_s / \Lambda_b$ is the reduced thickness. This expression assumes that phonons are diffusely scattered or emitted from the boundaries of the layer, which may slightly overestimate the conductivity reduction at low temperatures. Diffuse reflection results due to the interference of phonon wavepackets departing from an interface that has a characteristic roughness comparable to or larger than the phonon wavelength. The fraction of phonons reflected diffusely therefore depends strongly on the surface roughness and on the wavelength of the phonons under consideration. Partially specular reflection becomes more important at low temperatures. A more detailed analysis[9] considering partially specular reflection on boundaries with characteristic roughness 5 Å indicates that the resulting increase in the thermal conductivity is about 20% at 20 K for the 0.42 μm silicon overlayer.

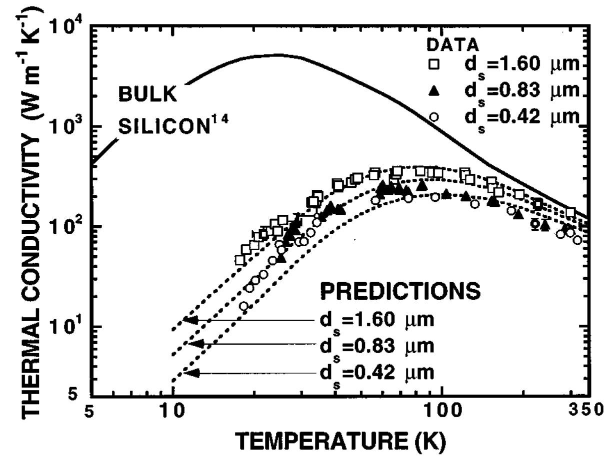

FIG. 2. Thermal conductivities of single-crystal silicon layers with thicknesses 0.42, 0.83, and 1.6 μm. Also included are recommended values for bulk silicon and predictions based on the phonon-boundary scattering analysis.

Figure 2 compares temperature-dependent thermal-conductivity data for silicon layers with the predictions of Eqs. (2) and (3) and with the recommended values for bulk samples.[14] The predictions use the conductivity model for bulk samples and the solution to the Boltzmann equation with no fitting parameters. The layer conductivities are strongly reduced compared to the bulk values, and the qualitative agreement with the data supports the conclusion that boundary scattering is responsible. The maximum in the conductivity for the thin layers occurs near 70 K and separates the low-temperature region, where scattering is dominated by imperfections and surfaces, from the high-temperature region, where phonon-phonon scattering is dominant. The bulk thermal conductivity reaches a maximum, 5500 W m^{-1} K^{-1} at a temperature near 30 K. Figure 2 shows that the data agree well with predictions for the 1.6-μm-thick silicon overlayer between 30 and 300 K. The effect of surface roughness is more significant at lower temperatures where the population of the long wavelength phonons increases. If partially specular reflection is considered,[9] the impact of phonon-boundary scattering below 30 K is significantly reduced and the agreement can be improved. The agreement for the 0.42- and 0.83-μm-thick silicon layers is somewhat poorer than for the thickest layer. This may be due to the higher concentrations of imperfections associated with epitaxial silicon growth in these layers. These imperfections tend to collect near the former interface with the heavily doped etch stop layer.[9,15]

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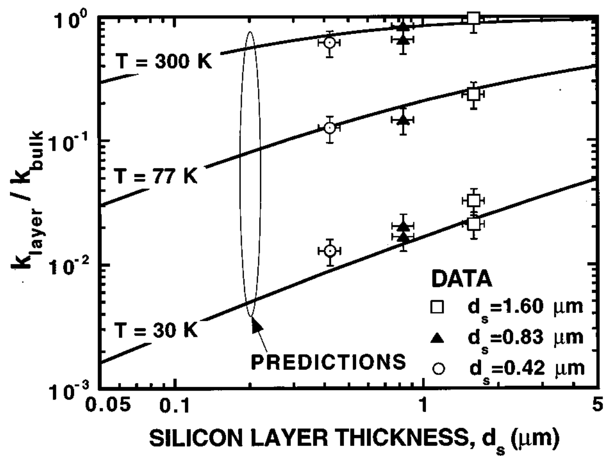

FIG. 3. Thermal conductivity reduction due to phonon-boundary scattering.

The impact of phonon-boundary scattering is demonstrated more clearly in Fig. 3, which plots the thermal conductivity reduction of the silicon layers compared to the recommended bulk values as a function of thickness and temperature. The predictions are consistent with the data except at low temperatures, where partially specular reflection may be responsible for the deviation. The reduction in thermal conductivity of the 1.6 μm sample is small and not experimentally significant at room temperature, suggesting a microstructure and purity that closely resemble those in bulk crystals. Figure 3 predicts that the size effect on the conductivity can exceed two orders of magnitude for layers of thickness near one micrometer at temperatures less than 10 K. This could be very important for low-temperature sensors made from single-crystal silicon layers. The predictions also indicate that the reduction could exceed 50% for layers thinner than 0.1 μm at room temperature, which has very important implications for the cooling of transistors in SOI circuits. For SOI transistors based on ultrathin device layers (less than 50 nm), the thermal conductivity could be reduced as much as 70%.

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[1] L. Peters, Semicond. Int. **16**, 48 (1993).
[2] K. E. Goodson, M. I. Flik, L. T. Su, and D. A. Antoniadis, ASME J. Heat Transfer, **117**, 574 (1995).
[3] B. W. Chui, T. D. Stowe, T. W. Kenny, H. J. Mamin, B. D. Terris, and D. Rugar, Appl. Phys. Lett. **69**, 2767 (1996).
[4] B. W. Chui, H. J. Mamin, B. D. Terris, D. Rugar, K. E. Goodson, and T. W. Kenny, International conference on Solid State Sensors and Actuators, Chicago, Illinois, IEEE **2**, 1085 (1997).
[5] Y. S. Ju and K. E. Goodson, Jpn. J. Appl. Phys. **36**, L798 (1997).
[6] C. H. Mastrangelo and R. S. Müller, Sens. Mater. **3**, 133 (1988).
[7] O. M. Paul, J. Korvink, and H. Baltes, Sens. Actuators A **A41**, 161 (1994).
[8] M. Von Arx and H. Baltes, J. Microelectromech. Syst. **1**, 193 (1992).
[9] M. Asheghi, M. N. Touzelbaev, K. E. Goodson, Y. K. Leung, and S. S. Wong, Presented at the Int. Mech. Eng. Congress and Exp., Atlanta, Georgia, November 17—22, DSC-**59**, in MEMS, C. T. Aredisian *et al.*, eds. **83** (1996). ASME J. Heat Transfer (in press). DSC-59, 83 (1996).
[10] K. E. Goodson, M. I. Flik, L. T. Su, and D. A. Antoniadis, IEEE Electron Device Lett. **14**, 490 (1993).
[11] Y. K. Leung, S. C. Kuehne, V. S. Huang, C. T. Nguyen, A. K. Paul, J. D. Plummer, and S. S. Wong, IEEE Electron Device Lett. **18**, 13 (1997).
[12] M. G. Holland, Phys. Rev. **132**, 2461 (1963).
[13] E. H. Sondheimer, Adv. Phys. **1**, 1 (1952).
[14] Y. S. Touloukian, R. W. Powell, C. Y. Ho, and P. G. Klemens, from *Thermophysical Properties of Matter* (IFI/Plenum, New York, 1970), Vol. 1, p. 339.
[15] W. P. Maszara, J. Electrochem. Soc. **138**, 341 (1991).

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