Heating Mechanisms of LDMOS and LIGBT in Ultrathin SOI

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Abstract—Temperature rises due to self-heating in silicon-on-insulator (SOI) power devices may lead to performance degradation and reliability problems. This letter investigates the mechanisms and spatial distribution of heat generation in linearly graded SOI LDMOS and LIGBT devices. While Joule heating dominates in LDMOS devices, hole collection at the p-well-drift region junction contributes strongly to the heating of LIGBT's. Also, the presence of both Joule and recombination heating makes the heating profile more uniform in LIGBT's. These effects combine to yield a temperature rise in LIGBT's that is more uniform and lower on average than that in LDMOS devices.

I. Introduction

SMART power technology [1], which integrates both logic and power devices on the same chip, is more readily implemented in silicon-on-insulator (SOI) substrates than bulk silicon substrates [2]. The buried oxide layer in SOI facilitates processing and provides electrical insulation but it also has a very low thermal conductivity. This impedes heat dissipation inside the device and increases peak temperature rise during operation [3]. This effect is more prominent in high voltage applications where very thin SOI and thick buried oxide layers are desired [4]. High-temperature rise caused by self-heating may degrade device performance and reliability.

The temperature distribution inside a device due to self-heating is determined by the heat generation profile and the thermal conduction inside the SOI film. Different power devices have different current conduction mechanisms and heat generation profiles. Thermal conduction is determined by structural parameters like the SOI layer thickness and the buried oxide thickness. If a thick SOI layer is used, the lateral thermal conduction inside the device will be quite effective and the temperature rise will be relatively uniform. In an ultrathin SOI film, lateral heat conduction is not very effective and the temperature in the device is closely linked to the heat generation profile. In this letter, the heating mechanisms and the resulting temperature profiles of LDMOS's and LIGBT's with a linearly graded doping profile in the drift region in thin SOI layers [5] are investigated.

II. Device Heating

Heat generation in semiconductor has been studied in detail [6]. A simplified model for the heat generation rate per unit volume is given by

$$H = \vec{J} \cdot \vec{E} + U E_g$$

where J is the current density, E the electrical field, U the recombination rate and E_g the bandgap of the semiconductor. The first term is the Joule heating caused by the electrical resistance associated with the semiconductor. Recombination of carriers also releases energy and gives rise to the second term. In majority carrier devices such as MOSFET's, there is very little carrier recombination and as a result heat generation is mainly from Joule heating. In p-n diodes and bipolar transistors, minority carrier injection is present and recombination heat generation is not negligible. Using a device simulator, the constituent heating terms can be investigated separately. Devices with cross-sections shown in Fig. 1 were simulated using the two-dimensional (2-D) simulator MEDICI with the lattice temperature advanced application module [7]. SOI thickness of 0.5 μm and buried oxide thickness of 3 μm were used. The 40-μm long drift region was doped linearly from 10^{15} cm^{-3} to 2.4×10^{17} cm^{-3}. The boundary conditions used are the same as the ones in [8]. In real circuit applications, the devices usually operate at a certain current level. With a much lower forward voltage drop, the LIGBT has a lower power dissipation and hence less of a self-heating problem in comparison with the LDMOS. To compare the different heating mechanisms in these two devices, however, the current levels are adjusted to achieve the same power dissipation of 1 W, or about 6 Wmm^{-2}, in this letter.

Heat generation rate per volume in the drift region of the LDMOS device is plotted in Fig. 2(a) together with the temperature distribution. Since LDMOS is a majority carrier device, only Joule heating is significant and it is proportional to the local resistance. The low dopant level near the source side of the drift region will give rise to a high heat generation rate. The irregularity of the heating profile at $x = 2$ μm is due to the polysilicon field plate above the field oxide. For $x < 0$ μm where the bird's beak of the LOCOS is located, there is actually heat absorption. This is due to the spreading of current which flows against the vertical electric field from the field plate. The increase in heat generation near the drain originates from the current crowding at the shallow n$^+$ junction. The finite lateral heat conduction in the thin SOI layer will make the gradient of the temperature profile less than that of the heat
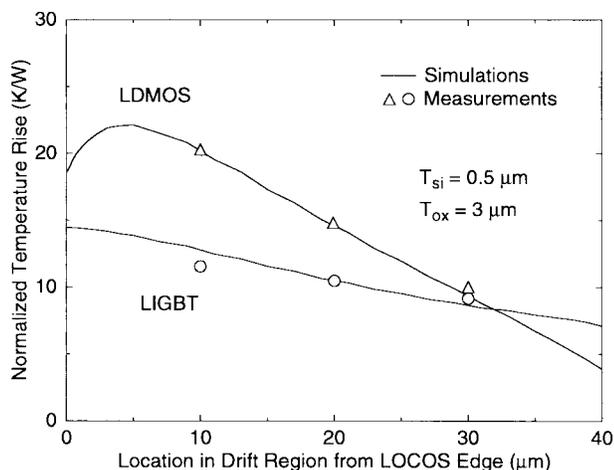
Fig. 1.   Schematic cross-sectional view of LDMOS and LIGBT devices. Derivation of the linearly graded doping profile can be found in [5].

Fig. 2.   Simulated heat generation and normalized temperature profiles in the drift regions of (a) LDMOS, and (b) LIGBT, built in 0.5-μm thick SOI layer on 3-μm buried oxide at 1 W of power dissipation. Constituent heat generation terms are plotted for the case of LIGBT.

generation but a high-temperature rise is still present near the source.

The LIGBT has a different heating profile as shown in Fig. 2(b). The individual heat components due to Joule heating and recombination heating are also plotted for analysis. Minority carrier injection from the p^+ collection leads to recombination heat which is highest near the collector and gradually decreases toward the emitter side. This is opposite to the trend of Joule heating and makes the total heat generation profile more uniform than in LDMOS's. Another difference is that a large portion of the power is in fact not dissipated in the thin drift region, but at the reverse-biased junction formed

by the p-well and the n^- drift region. When the holes are collected by the p-well, the aligned current flow with the high electric field in the depletion region gives rise to a large amount of energy released. This shift of peak power dissipation in the LIGBT toward the emitter metallization eases heat conduction and helps reducing the maximum temperature rise in the device. A lower and more uniform temperature rise in the LIGBT thus results.

III. EXPERIMENTS

The temperature profiles in the drift regions of the devices were experimentally measured using a resistance thermometry

Fig. 3. Experimentally measured temperature rises in the drift regions of LDMOS and LIGBT devices built in 0.5-μm thick SOI layer on 3-μm buried oxide together with simulated temperature profiles.

technique as described in [8]. LDMOS and LIGBT devices were built in SOI wafers prepared by wafer bonding and etchback. Fabrication process including the implementation on the linearly graded dopant profile in the drift region was described in [9]. A 4-μm wide polysilicon resistor laid out as a four-point structure over the drift region was used as a thermistor. By placing the polysilicon thermistor at 10, 20, and 30 μm from the LOCUS edge, a coarse spatial temperature profile of the device could be obtained. The behavior of the thermistor with temperature was first characterized using a hot chuck. The actual temperature of the device was then obtained by monitoring the resistance of the thermistor during operation.

The measured temperature profiles of the LDMOS and the LIGBT are plotted in Fig. 3 and they agree well with the simulated profiles. There is a large temperature gradient in the drift region of the LDMOS, but the temperature distribution is much more uniform in the LIGBT.

IV. CONCLUSIONS

In summary, the heating mechanisms of LDMOS and LIGBT devices built in thin SOI layers have been investigated. 2-D electrothermal simulations have been used to understand the temperature profiles in these devices. For LDMOS devices with a linearly graded dopant profile in the drift region, the part near the source is more resistive, which results in a higher heat generation rate and thus a larger temperature rise. For the case of LIGBT, the combination of Joule and recombination heat makes the heat generation more uniform across the drift region. In addition, a large fraction of the power is dissipated at the p-well-drift region junction, where cooling by the nearby emitter metallization is more effective. These effects reduce the temperature rise and gradient in the device.

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