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Size Effect on Thermal Conduction in Silicon-on-Insulator Devices under Electrostatic Discharge (ESD) Conditions

Yongho Sungtaek JU and Kenneth Eugene GOODSON
Department of Mechanical Engineering, Stanford University, Stanford, CA 94305-3030, USA

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Previous experimental work has shown degradation in the electrostatic discharge (ESD) failure voltage for silicon-on-insulator (SOI) devices compared to that of devices made from bulk silicon substrates. Understanding of this trend requires simulations of temperature fields in SOI devices using accurate thermal property values. The present work predicts the in-plane lattice thermal conductivity of thin silicon films at temperatures up to 1000 K considering the size effect due to phonon-boundary scattering. For silicon layers thinner than 0.2 μm, a significant reduction in the thermal conductivity is expected even at temperatures as high as 700 K. A compact expression for the thermal conductivity of thin silicon films can be readily used in device simulations. Temperature field predictions for a simplified SOI device show the impact of the size effect and motivate discussion of its implications for ESD buffer design.

KEYWORDS: SOI devices, thermal conductivity, size effect, electrostatic discharge (ESD)

1. Introduction

The failure of semiconductor devices during electrostatic discharge (ESD) is closely related to the resulting temperature rise.[1] The current localization, which is believed to occur when the temperature rise in devices exceeds a critical value, leads to extremely high heat generation density and ultimately to failure.[2] The problem is more acute for SOI devices due to the low thermal conductivity of the buried silicon dioxide layer.[3] Careful circuit and layout designs are necessary to achieve acceptable failure threshold voltages,[4] which can be greatly facilitated by accurate knowledge of temperature fields in the devices. Although heat conduction along thin silicon device layers plays a crucial role in determining the temperature rise in SOI devices,[5] the high temperature thermal conductivity of thin silicon layers needed for ESD simulations has received little attention.

In silicon, heat is transported predominantly by phonons, which are the energy quanta of lattice vibrations. When the mean free path of phonons becomes comparable with the thickness of a film, the thermal conductivity is reduced from the bulk value due to phonon-boundary scattering. The impact of this size effect on the thermal conductivity of thin silicon layers was studied in connection with the packing limit of SOI transistors at low temperatures, where the phonon mean free path can be on the order of a few micrometer and the size effect is more pronounced.[6] Recently, there also were measurements of the in-plane thermal conductivity of sub-micrometer thick silicon layers at and below room temperature.[7] Corresponding study on the high temperature thermal conductivity of thin silicon layers has not been reported. This size effect is expected to be augmented by the highly dispersive nature of the phonon spectrum in silicon.

In this manuscript, we use an existing thermal conductivity model of silicon to predict the in-plane thermal conductivity of thin silicon layers. A compact expression derived from a simplified analysis is also given, which can be readily incorporated into device simulations. Temperature field predictions for a simplified SOI device show the impact of the size effect and motivate the discussion of its implication for ESD buffer design.

2. Thermal Conductivity of Thin Silicon Layers

Detailed theoretical study of the thermal conductivity of bulk silicon has considered the nonlinear phonon dispersion relations.[8,9] The theory yielded a thermal conductivity integral, which summed the contribution to thermal conductivity from phonons of all available frequencies. Anharmonic interactions among lattice waves and crystal defects are the main sources of thermal resistance in bulk silicon at high temperatures. The theoretical model of Holland,[8] which is used in this study, reproduced the experimental data up to 1200 K, which is near the melting point of silicon. The size effect can be considered using a solution to the Boltzmann transport equation, which relates the in-plane conductivity of a thin film to that of a bulk material.[10] The energy dependence of phonon scattering and phonon dispersion can be considered together with the size effect by incorporating the Boltzmann equation solution into the bulk silicon thermal conductivity model.

Figure 1 shows the ratio between the predicted values of the thermal conductivity of silicon films, k_{film}, and the bulk values, k_{bulk}, as a function of temperature for several different silicon film thicknesses. Diffuse scattering of phonons at interfaces between silicon and silicon dioxide layers is assumed. This is justified by the fact that the dominant phonon wavelength is comparable to one nanometer, which is comparable to the characteristic roughness of the interface, and also by the fact that those phonons transmitted into amorphous silicon dioxide layers are diffusely re-emitted after undergoing scattering within the silicon dioxide layers. Recommended values of Touloukian *et al.*[11] are used for the high temperature thermal conductivity of bulk silicon. As temperature increases, the bulk mean free path of phonons becomes smaller, diminishing the relative impact of the size effect. The reduction in the thermal conductivity, however, is significant even at relatively high temperature

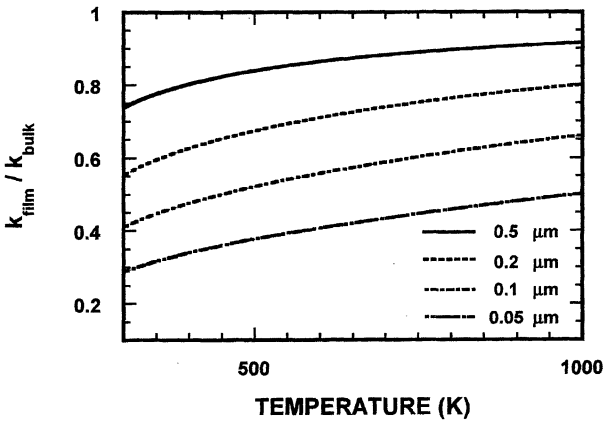

Fig. 1. The ratio between the thermal conductivity of thin films of pure or moderately doped silicon, k_{film}, and the bulk conductivity, k_{bulk}, as a function of temperature for various film thicknesses.

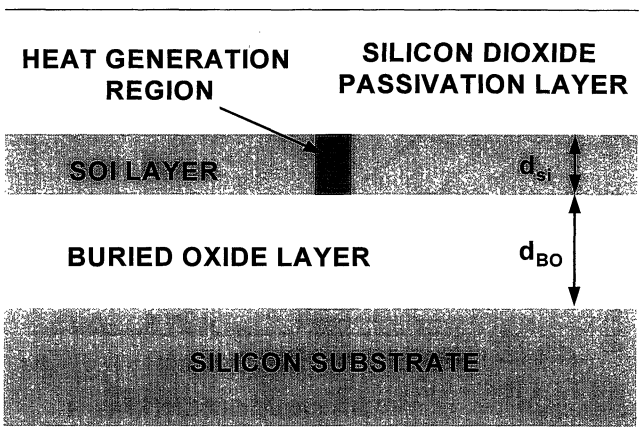

Fig. 2. Schematic of the model SOI device structure studied.

for films thinner than 0.2 μm. For heavily-doped silicon with doping concentration near 10^{20} cm^{-3}, the bulk thermal conductivity and, hence, the bulk mean free path of phonons can be smaller than those of pure or moderately doped silicon.[11] As a result, the size effects is expected to be less pronounced for heavily doped silicon especially at low temperatures.

A simplified approach, which does not require numerical evaluation of the thermal conductivity integral, is also possible. This approach uses as a key parameter the mean free path of phonons in bulk samples denoted by λ_{bulk}, which can be estimated from the bulk thermal conductivity, k_{bulk}, using the relation

$$k_{bulk} = \frac{1}{3} C v \lambda_{bulk}. \quad (1)$$

Here C and v are the weighted average values of the heat capacity and the propagation velocity of those phonons participating in the heat conduction.

In this study, following the suggestion of a previous research,[8] the transverse acoustic phonon spectrum is modeled to consist of three linear segments with different slopes and, hence, different group velocities. For silicon the transverse acoustic phonons over a small region in the first Brioullin zone was suggested to carry most of heat at near or above room temperature. The mean heat capacity of these phonons can be approximately obtained following the approach similar to the Debye theory,[12] yielding

$$\frac{1}{3} C v = 1.13 \times 10^{13} \frac{\exp(195/T)}{T^2(\exp(195/T)-1)^2} [\mathrm{W \cdot m^{-2} \cdot K^{-1}}]. \quad (2)$$

The in-plane thin film thermal conductivity, k_{film}, can be obtained from the formula[10]

$$k_{film} = \frac{(1/3)Cv}{(1/3)Cv/k_{bulk} + 3/(8d)}, \quad (3)$$

which is an approximation to a more complete formula available.[10] Equation (3) provides good approximation for all the cases examined here. The error resulting from the use of the approximate formulas eqs. (2) and (3) is less than 15% for temperatures above 300 K.

3. Temperature Fields in SOI Devices

To assess the consequence of the thermal conductivity reduction on temperature fields in SOI devices, transient temperature fields in a model structure are calculated by solving the two dimensional transient heat conduction equation. A schematic of a model structure is shown in Fig. 2. A constant-amplitude heating pulse of duration 100 ns is assumed to induce heating at a localized region with the length 120 nm, such as a high-field region near drain diffusions of field-effect transistors. The solution domain includes passivation oxide, SOI and buried oxide layers. The SOI layer is assumed to be moderately doped such that the thermal conductivity reduction due to heavy doping is negligible. The thickness of the passivation oxide layer is assumed to be larger than the heat diffusion length, which is on the order of 0.3 μm. The bottom boundary condition for the buried oxide layer is assumed to be isothermal, which is justified by the short-duration of the pulse and the high thermal conductivity of the silicon substrate. The other boundaries are assumed to be adiabatic. Thermal properties are evaluated at 500 K,[11] which is the mean value of room temperature and 700 K, the intrinsic temperature of silicon with doping concentration around 5x10^{16} cm^{-3}. The intrinsic temperature of silicon has been suggested to be the critical temperature associated with the second-breakdown and, hence, failure under ESD.[1]

Since the thickness of the buried oxide layer, d_{BO}, is smaller than the thermal diffusion length for the timescale examined, the reduced-temperature rise is expected to be roughly inversely proportional to the square root of the thickness of SOI layers similar to the steady-state case.[5] Figure 3 compares the maximum values of temperature rises per unit power dissipated and per unit width of the structure, which are calculated using the predicted and the bulk values of the thermal conductivity of SOI layers. The difference between the two results increases with decreasing SOI thickness, which can reach up to 30 % for the thinnest layer examined.

The simulation results are in qualitative agreement with the existing experimental data,[3] where the ESD failure voltage of SOI multi-finger nMOSFET's was observed to drop more sharply with decreasing silicon film

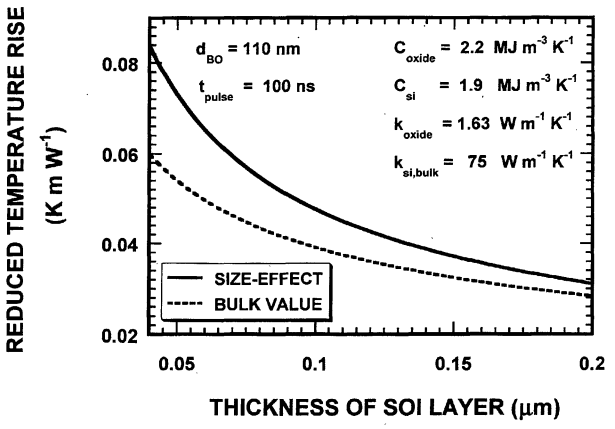

Fig. 3. Comparison of the maximum values of the temperature rise in the model structure calculated using the predicted thin film thermal conductivity and the bulk value.

thickness for ultra-thin SOI devices. The overprediction of power-to-failure values of SOI transistors reported in a recent theoretical study [13] can also be partly explained by the size effect. In addition, better agreement with experimental results can be achieved when the size effect on thermal conductivity is taken into account in predicting the steady state temperature rise of single gate SOI MOSFET's under normal operating conditions.[5,14] Quantitative comparison with the experimentally measured ESD failure voltages, however, is difficult due to the lack of precise knowledge on the failure mechanisms and also non-uniform turn-on behavior for the case of multi-finger MOSFET's.

4. Implications for ESD Buffer Transistor Design

One of the important parameters in designing ESD buffer transistors is the gate-to-contact spacing.[1] This is especially important for non-silicided devices, since failure can occur at diffusion contacts at temperatures much lower than the silicon melting temperature. The gate-to-contact spacing is also a key to the optimization of multi-finger structures to reduce the area they occupy.

For SOI devices with ultra-thin silicon device layers, the lateral flow of heat is more restrained than in devices with thicker device layers due to the thermal conductivity reduction resulting from the size effect as well as due to a smaller volume of silicon available for heat conduction. This is consistent with the experimental observation that silicon melting preceded aluminum melting for most cases.[3] The extent of lateral heat flow can be roughly estimated to be the thermal decay length,[5] $\sqrt{d_{Si} d_{BO} k_{film}/k_{BO}}$, which ranges from 0.25 to 0.85 μm for the cases examined in the present work.

5. Summary and Conclusion

The degradation of the ESD failure voltage of SOI devices has been attributed to the high thermal resistance of SOI devices compared to that of their bulk counterparts. In this manuscript, the high temperature in-plane thermal conductivity of thin silicon layers is studied theoretically. This conductivity is one of the key parameters that govern temperature rise in SOI devices. A compact formula relating the thin film thermal conductivity values to the bulk value is also derived. A significant reduction in the thermal conductivity is predicted even at high temperatures for moderately doped silicon films of thickness smaller than 0.2 μm. Further experimental as well as theoretical work is needed in connection especially with the size effect on the thermal conductivity of heavily doped silicon films.

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