# Scaling Analysis of Multilevel Interconnect Temperatures for High-Performance ICs

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***Abstract*—This paper presents a comprehensive thermal scaling analysis of multilevel interconnects in deep nanometer scale CMOS technologies based on technological, structural, and material data from the International Technology Roadmap for Semiconductors. Numerical simulations have been performed using three-dimensional electrothermal finite element methods, combined with accurate calculations of temperature- and size-dependent Cu resistivity and thermal conductivity of low-$\kappa$ interlayer dielectrics (ILD) based on fully physical models. The simulations also incorporate various scaling factors from fundamental material level to system level: the via-density-dependent effective ILD thermal conductivity, the hierarchically varying root mean square current stress based on SPICE simulations, and the thermal resistance of flip-chip package. It is shown that even after considering densely embedded vias, the interconnect temperature is expected to increase significantly with scaling, due to increasing current density, increasing surface and grain boundary contributions to metal resistivity, and decreasing ILD thermal conductivity.**

***Index Terms*—Electrothermal analysis, interconnects, Joule heating, low-$\kappa$ dielectrics, metal resistivity, size effect, temperature scaling, very large-scale integrated system (VLSI), via effect.**

## I. Introduction

ACCURATE estimates of multilevel interconnect temperatures are necessary for interconnect performance and reliability assessment in high-performance very large-scale integrated (VLSI) circuits [1]–[3]. While some analytical thermal models are available for multilevel interconnects, the complicated multidimensional heat conduction within the three–dimensional (3-D) interconnect structures are either neglected or treated approximately [4]–[7]. Previous thermal simulations for multilevel interconnects often assumed simplified structures with arbitrary dimensions and material systems: all parallel lines in $SiO_2$ or polyimide [8] and only three- to four-level orthogonal wires in $SiO_2$ [9], [10]. Rigorous thermal analysis of multilevel interconnects must consider complex 3-D thermal coupling caused by orthogonal interconnect arrays, densely embedded vias, increasing number of metal levels, material property variations, and nonuniform current stress conditions.

This paper significantly improves upon our previous work [11] by including temperature- and size-dependent Cu resistivity, effective ILD thermal conductivity accounting for both varying via densities and via Joule heating, package thermal resistance scaling for high I/O chips, and realistic metal-level-dependent root mean square current stress inputs. The predictions made for interconnect temperatures can be used for investigating highly coupled electrothermal phenomena resulting from material property and physical parameter scaling dictated by technology evolutions. These results can also be used for enhancing backend thermal management, performance, and reliability, and for incorporating thermal-awareness in interconnect design issues such as power/ground distribution network and clock design.

The paper is organized as follows. Section II examines the scaling physics of Cu resistivity and low-$\kappa$ thermal conductivity. Section III addresses detailed methodologies for the accurate simulations based on finite element methods (FEM) including via density and flip-chip package effects. In Section IV, a scaling analysis of the multilevel interconnect temperature is presented along with discussion. Finally, concluding remarks are made in Section V.

## II. Material Property Scaling

### A. Cu Resistivity

The metal resistivity increase due to size effects is an emerging concern as the width of on-chip interconnects approaches the mean-free path of electrons (about 40 nm for Cu at room temperature). The compact analytical model in [12] is used to calculate the resistivity of rectangular wires, which is based on the Fuchs–Sondheimer model [13], [14] regarding surface scattering and the Mayadas–Shatzkes model [15] regarding grain boundary scattering of electrons

$$\rho = \rho_o \left\{ \frac{\frac{1}{3}}{\left[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)\right]} + \frac{3}{8} C (1-p) \frac{1+AR}{AR} \frac{\lambda}{w} \right\}$$
$$\alpha = \left(\frac{\lambda}{d_g}\right)\left[\frac{R}{(1-R)}\right] \quad (1)$$

where $\rho_o$ is the bulk resistivity, $\lambda$ is the mean free path of electrons, $w$ is the metal width, AR is the aspect ratio (height over width), $p$ is the specularity parameter, $R$ is the reflectivity coefficient at grain boundaries, $d_g$ is the average distance between grain boundaries, and $C$ is a constant (1.2 for rectangular cross sections). The accuracy of this model compared to the integral

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expression used in [16] is better than 3.5% for 50 nm $< w <$ 1000 nm [12].

In bulk materials, the grain-boundary contribution to the resistivity is small because the grain size is usually much larger than the mean free path of electrons. However, the grain size is reduced in thin films and wires, which is comparable to or smaller than the mean free path [15]. Therefore, electron scattering at the grain boundaries must be considered in wires as well as scattering at the external surfaces. The grain size in narrow Cu wires fabricated by an electrochemical process is limited by the lateral dimensions of wires and shown to increase linearly with the metal width for $w < 230$ nm and AR $> 1$ [12]. Therefore, $d_g$ can be replaced by $w$ in (1) for calculating the resistivity of metal wires based on the International Technology Roadmap for Semiconductors (ITRS) ($w = 22-185$ nm, AR $=$ 1.9$-$2.7). It is important to note that $w$ and AR in (1) correspond to the actual conducting area of Cu, which excludes highly resistive thin barrier layers at the bottom and the side walls of the Cu conductor. The technology roadmap predicts that the barrier layer occupies a significant fraction of the drawn metal area: 22–23% for metal 1 (M1), 18–19% for intermediate wires, and 12% for global wires. Therefore, the barrier layer effect must be included in resistivity calculations by using corrected $w$ and AR from the ITRS specified drawn wire dimensions and barrier layer thickness. Other parameters are average values based on [12]: $\rho_o = 2.04\ \mu\Omega \cdot \mathrm{cm}$ (300 K), $\lambda = 37.3$ nm (300 K), $p = 0.41$, and $R = 0.22$.

The temperature- and size-dependent resistivity values are calculated for M1, intermediate, and global wires at each technology node using (1) with ITRS dictated parameters at each technology node and with temperature-dependent parameters ($\rho_o$ and $\lambda$) known at a given temperature. Note that only $\rho_o$ and $\lambda$ change with temperature and other scattering parameters ($p$ and $R$) are independent of temperature. As temperature increases, $\rho_o$ increases linearly and $\lambda$ decreases satisfying $\rho_o \times \lambda =$ constant [16]. The calculated resistivity and its constituents are shown in Fig. 1 as a function of technology node for the ITRS intermediate wires at 300 K. In advanced technology nodes, $\rho$ is expected to increase significantly above $\rho_o$ mainly due to the enhanced surface and grain boundary scattering. The contribution of surface scattering and grain boundary scattering is roughly the same, but both increase with scaling. The background scattering of the electrons by phonons, electrons and defects (impurities) that contributes to $\rho_o$ remains constant at a given temperature, independent of scaling (wire dimensions).

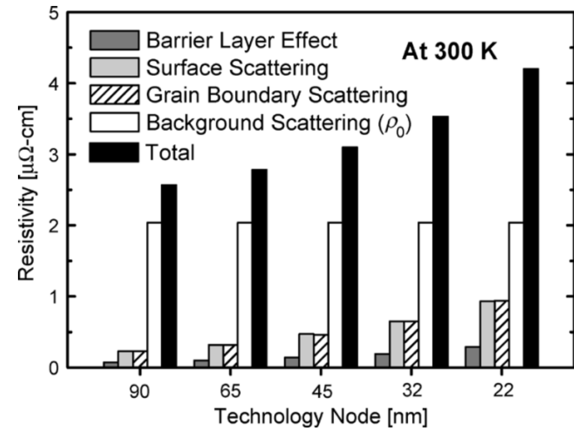


Fig. 1. Scaling of Cu resistivity for the ITRS intermediate wires at 300 K. The total resistivity is the sum of all the resistivity increments $\Delta\rho_s$, $\Delta\rho_g$, and $\Delta\rho_b$ due to surface scattering, grain-boundary scattering and barrier layer effect, plus the bulk resistivity ($\rho_0$). The increments, $\Delta\rho_s(= \rho_s - \rho_0)$ and $\Delta\rho_g(= \rho_g - \rho_0)$ can be easily estimated from (1) using the ITRS specified drawn wire dimensions, where the first and second terms correspond to $\rho_g$ and $\Delta\rho_s$, respectively. The increment due to barrier layer $\Delta\rho_b$ $(= \rho_b - \rho)$ can also be estimated from (1), where $\rho_b$ is the resistivity estimated from (1) based on the actual metal conducting dimensions excluding barrier layers and $\rho$ is the resistivity based on the drawn wire dimensions.

## B. Thermal Conductivity of Low-$\kappa$ Dielectrics

The low-$\kappa$ dielectric materials for interlayer and intermetal dielectric (ILD and IMD) applications are expected to have much lower thermal conductivities than oxide. It is important to assess the correlation between thermal conductivity and dielectric constant in order to evaluate the tradeoff between electrical and thermal performance. While the ITRS specifies the dielectric constant of ILD ($k_{\mathrm{ILD}}$) at each technology node, the thermal conductivity of ILD ($K_{\mathrm{ILD}}$), one of the essential material properties for electrothermal FEM simulations, is not available. It is difficult to find a universal relationship between $K_{\mathrm{ILD}}$ and $k_{\mathrm{ILD}}$ encompassing all low-$\kappa$ dielectric candidates owing to the intrinsic differences in their compositions and structures.

The relationship between $K_{\mathrm{ILD}}$ and $k_{\mathrm{ILD}}$ can be found if a dielectric material is porous. Using the Bruggemann effective medium theory [17], the $k_{\mathrm{ILD}}$ is expressed as

$$P\left(\frac{k_p - k_{\mathrm{ILD}}}{k_p + 2k_{\mathrm{ILD}}}\right) + (1-P)\left(\frac{k_m - k_{\mathrm{ILD}}}{k_m + 2k_{\mathrm{ILD}}}\right) = 0 \quad (2)$$

where $P$ is the porosity $(0 < P < 1)k_p$, is the dielectric constant of pores, and $k_m$ is the dielectric constant of a matrix material. The thermal conductivity of a porous dielectric material can be obtained from several models such as the parallel model, the serial model, the dilute particle model, the dilute fluid model, the porosity weighted dilute medium model, the porosity weighted simple medium (PWSM) model [18], [19], and the differential-effective-medium (DEM) model [20]. The PWSM model for $K_{\mathrm{ILD}}$ is given by

$$K_{\mathrm{ILD}} = [PK_p + (1-P)K_m](1-P^x) + \frac{K_p K_m P^x}{PK_m + (1-P)K_p} \quad (3)$$

where $K_p$ is the thermal conductivity of pores, $K_m$ is the thermal conductivity of a matrix material, and $x$ is the fitting parameter. Calculating $K_{\mathrm{ILD}}$ and $k_{\mathrm{ILD}}$ by continuously varying $P(0 < P < 1)$ numerically yields the relationship between these two properties for a given porous dielectric material.

Fig. 2 shows the correlation between thermal conductivity and dielectric constant of ILDs. The predictions based on the DEM and PWSM models for porous silicate (xerogel) films are plotted with experimental data from literature for various low-$\kappa$ candidates including xerogel: fluorinated silicate glass (FSG) [21], hydrogen-silsesquioxane (HSQ) [20], [22], carbon-doped oxide (CDO) [21], [22], organic polymers [22], methyl-silsesquioxane (MSQ) [23], and xerogel [20], [24], [25]. For the ITRS specified range of dielectric constant ($k_{\mathrm{ILD}} < 3$), the PWSM model fits better with experimental data for xerogel:

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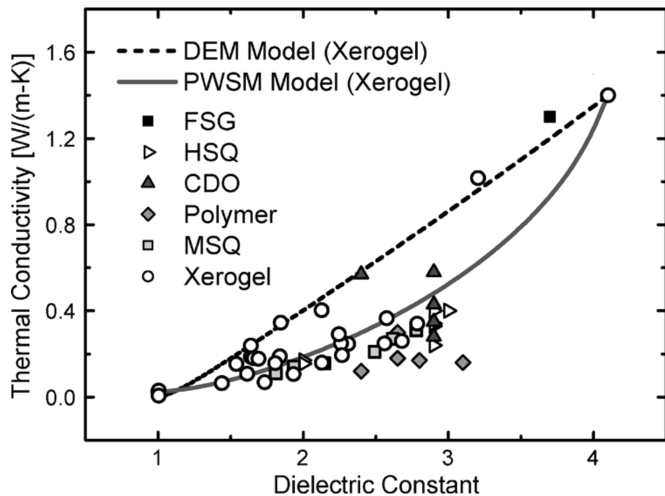


Fig. 2. Correlation between thermal conductivity and dielectric constant. The DEM and PWSM models for xerogel films are calculated using parameters $k_p = 1$, $k_m = 4.1$, $K_p = 0.0255$ W/(m-K), $K_m = 1.4$ W/(m-K), and $x = 0.49$ [18]. $P$ is varied continuously from 0 to 1. $P = 0$ yields properties of a fully dense material (silicate) and $P = 1$ those of air.

root-mean-square-errors are 0.08 and 0.22 W/(m-K) for the PWSM and DEM models, respectively. Although the PWSM model is plotted for xerogel, it can be used as a reasonable upper bound of $K_{\rm ILD}$ for other low-$\kappa$ dielectrics. We extracted the required $K_{\rm ILD}$ values corresponding to the ITRS specified bulk $k_{\rm ILD}$ values by using (2) and (3) with $0.357 < P < 0.668$ and parameters for xerogel.

## III. FEM Simulations

### A. Via Effects

The vias and contacts can be efficient heat dissipation paths from the upper level interconnects to the Si substrate and heat sink because they have much higher thermal conductivities than that of the ILD layers. On the other hand, since these electrical vias and contacts carry current, they also generate heat within their structures and increase the temperature of metal lines connected to them. Accurate estimates of interconnect temperature rise must consider these two opposite effects of vias [26]. The thermal impact of vias can be quantitatively represented by the effective thermal conductivity of ILD layers $(K_{\rm ILD,eff})$, [7], [27]. The $K_{\rm ILD,eff}$ value strongly depends on the via density in each ILD layer, which is typically higher for local levels and lower for global levels.

For a periodic array of metal lines and vias in Fig. 3(a), a unit cell can be defined as the volume between the symmetry planes in Fig. 3(b). Considering heat dissipation from the sides of metal lines, the effective width where thermal conduction takes place is assumed to be the entire width of the unit cell $(= w + d)$, where $d$ is the metal spacing. Constructing an equivalent 1-D thermal circuit for the unit cell results in

$$K_{\rm ILD,eff} = f \cdot K_V + (1 - f)K_{\rm ILD} \tag{4}$$

$$f = \frac{X^2}{[(w + d)L]} \tag{5}$$

where $f (0 < f < 1)$ is the via density defined as the ratio of the via volume to the ILD volume within the unit cell, as illustrated

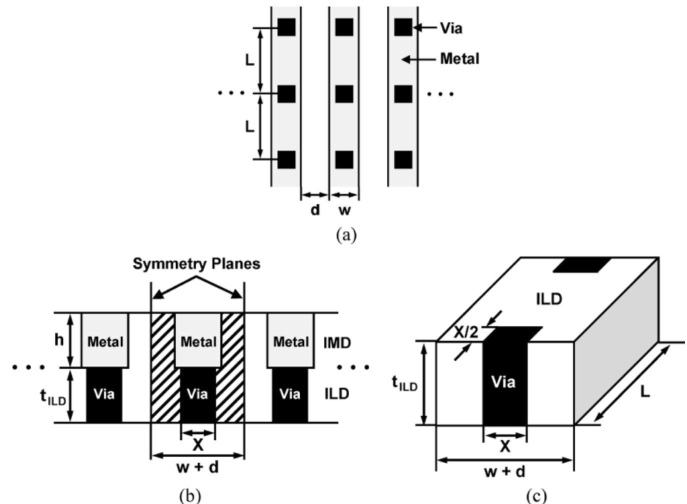


Fig. 3. Schematic of a periodic array of metal lines and vias: (a) layout, (b) cross section, and (c) the volume defining the via density.

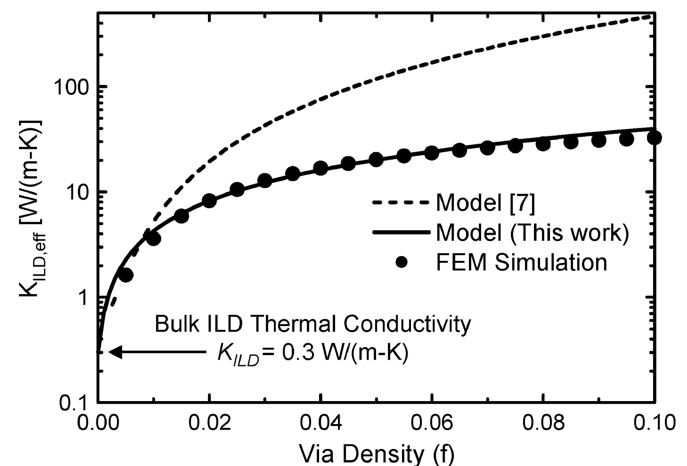


Fig. 4. Effective thermal conductivity of ILD layers $(K_{\rm ILD,eff})$ as a function of via density $(f)$. Simulation parameters are based on metal 1 (M1) of 65-nm technology node: $w = d = X = 76$ nm, $h = t_{\rm ILD} = 129.2$ nm, $K_{\rm ILD} = 0.3$ W/(m-K), $K_M = K_V = 396.36$ W/(m-K), $J = 3$ MA/cm$^2$, $\rho = 5.75\ \mu\Omega \cdot$ cm, and the reference temperature is 85 °C.

in Fig. 3(c), $K_V$ is the via thermal conductivity, $X$ is the via size, and $L$ is the intervia distance along the metal line. The via size $X$ is assumed to be the same as the minimum line width connected to the via.

In order to evaluate this analytical model for $K_{\rm ILD,eff}$, 3-D electrothermal FEM simulations are performed for the unit cell in Fig. 3(b) with varying $L$. The metal line and via carry the same current, and the IMD layer is assumed to be the same as the ILD layer. Fig. 4 compares the $K_{\rm ILD,eff}$ values extracted from FEM simulations with the predictions from thermal models as a function of $f$. The $K_{\rm ILD,eff}$ values are extracted from FEM simulations by $K_{\rm ILD,eff} = (J^2\rho \cdot h \cdot t_{\rm ILD})/\Delta T_{\rm avg}$, where $J$ is the current density in the metal line, $h$ is the metal height, $t_{\rm ILD}$ is the ILD thickness, and $\Delta T_{\rm avg}$ is the average temperature rise of the metal line with respect to the bottom surface of the unit cell. It is shown that the $K_{\rm ILD,eff}$ using (4), (5) fits better with the FEM simulation results. A previous model [7], which neglects heat dissipation from the sides of metal lines and heat generation in the vias themselves, significantly overestimates $K_{\rm ILD,eff}$ especially for the higher via densities. In this paper,

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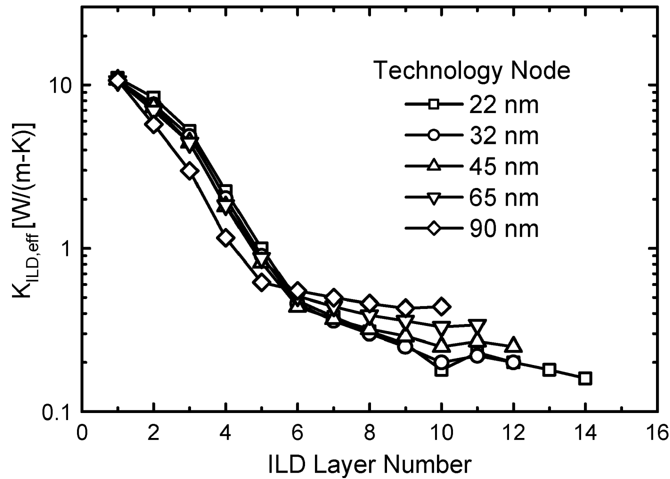


Fig. 5. Effective thermal conductivity of ILD layers $(K_{\mathrm{ILD,eff}})$ as a function of ILD layer number for different technology nodes. The $n^{\mathrm{th}}$ ILD layer is defined as the ILD layer between the $(n-1)^{\mathrm{th}}$ and $n^{\mathrm{th}}$ metal levels from the substrate.

(4), (5) are used for calculating metal-level-dependent $K_{\mathrm{ILD,eff}}$ at each technology node.

The via density $(f)$ or intervia distance $(L)$, which is not provided by the ITRS, varies with metal level depending on various circuit design parameters. In this work, we propose reasonable $L$ values at successive metal levels using the following criteria. For local (M1) wires, $L$ is taken as the typical local interconnection length which is roughly 2–3 times the source/drain diffusion length of a minimum sized NMOS. For intermediate wires, the metal wire at the center of intermediate tier (M5 for 90-nm node and M6 for the other nodes) is assumed to have an intervia distance equal to the typical length of intermediate level interconnections. For the topmost global wire, the typical interbuffer distance (hence $L$) for optimal delay in the longest global wires at the current technology node (90-nm node) is taken as 1 mm, and for future technology generations this length is scaled in accordance with wire width scaling. For the remaining successive metal levels, the $L$ values are assigned by linear interpolations on a log scale.

Using these metal-level-dependent $L$ values, the $f$ values are calculated by using (5) assuming $d = w$, and then the $K_{\mathrm{ILD,eff}}$ values are calculated by using (4). For the first ILD layer that is the premetal dielectric (PMD) layer, we assumed phospho silicate glass (PSG) as a PMD material and tungsten as a contact material with thermal conductivities of 0.94 W/(m-K) [28] and 165 W/(m-K) [29], respectively. In Fig. 5, it is shown that the $K_{\mathrm{ILD,eff}}$ values of lower ILD layers become much higher than the bulk ILD thermal conductivity, $K_{\mathrm{ILD}} = 0.12 - 0.4$ W/(m-K), due to densely embedded local vias. In the FEM simulations, these $K_{\mathrm{ILD,eff}}$ values are parametrically assigned to each ILD layer as material properties, which effectively include vias with varying densities.

### B. Package Effects

Heat dissipated from the multilevel interconnect stacks is often assumed to be removed through the Si die, integrated heat spreader (IHS) and heat sink by neglecting heat dissipation through the package layers to the printed-circuit board (PCB) [11]. Fig. 6 shows schematic of a standard flip-chip controlled collapsed chip connection (C4) package. The topmost global interconnects covered by passivation layers are successively attached to the (solder bumps + underfill) layer, package substrate, solder balls, and PCB. Unlike our previous work [11], we effectively include heat dissipation through the package layers in our simulations by adding an equivalent package layer with thermal resistance of $R_{\mathrm{th,eq}}$ to the topmost global wires

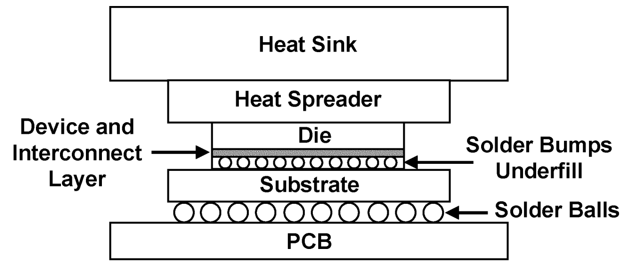


Fig. 6. Schematic of flip chip C4 package.

$$R_{\mathrm{th,eq}} = \sum_i R_{\mathrm{th,i}} = \sum_i \left(\frac{t_i}{K_i}\right) \tag{6}$$

where $i$ represents each package layer from passivation layers to PCB, $R_{\mathrm{th,i}}$ is the thermal resistance $(\mathrm{mm^2K/W})$, $t_i$ is the thickness, and $K_i$ is the thermal conductivity of the $i^{\mathrm{th}}$ package layer, respectively.

For the (solder bumps + underfill) layer, the effective thermal conductivity $(K_{U,\mathrm{eff}})$ at each technology node is calculated using the 1-D thermal circuit model and ITRS specified area array flip chip package requirements for high-performance microprocessor units (MPUs) as follows:

$$K_{U,eff} = \phi \cdot K_B + (1-\phi) K_U \tag{7}$$

$$\phi = \frac{N_B W_B^2}{A_c} \tag{8}$$

where $\phi$ is the volume fraction of solder bumps $(0 < \phi < 1)$, $K_B$ is the thermal conductivity of solder bumps $(= 36\ \mathrm{W/(m \cdot K)}$ [30]), $K_U$ is the thermal conductivity of underfill layer $(= 0.6\ \mathrm{W/(m \cdot K)}$ [30]), $N_B$ is the number of solder bumps, $W_B$ is the width of the solder bumps, and $A_c$ is the chip area. The calculated $K_{U,\mathrm{eff}}$ values are 1.41–2.57 $\mathrm{W/(m \cdot K)}$, which are within the range of published values [30]–[32]. For the other package layers, we use thickness and thermal conductivity values in Table I to calculate the thermal resistance $R_{\mathrm{th,i}}$ in each layer. The impact of (solder bumps + underfill) layer scaling is found to be negligible, overwhelmed by the huge thermal resistances of other package layers such as the solder ball/air layer and PCB. The calculated $R_{\mathrm{th,eq}}$ values are two orders of magnitude higher than the junction-to-ambient thermal resistances (toward the heat sink). Therefore, most heat dissipated from the multilevel interconnects is expected to be removed through the Si die, IHS, and heat sink.

### C. FEM Simulation Methodology

The 3-D electrothermal FEM simulations are performed by ANSYS to account for temperature-dependent Joule heating of

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TABLE I
THICKNESS, THERMAL CONDUCTIVITY, AND THERMAL RESISTANCE OF PACKAGE LAYERS

| Layer | Thickness (mm) | $K$ (Wm$^{-1}$K$^{-1}$) | $R_{th}$ (mm$^2$K/W) | Reference |
|---|---|---|---|---|
| Passivation (TEOS) | 0.001* | 1.4 | 0.71 | [21] |
| Passivation (SiN) | 0.001* | 2.23 | 0.45 | [28] |
| Solder Bump | 0.0762 | 36 | 2.12 | [30] |
| Underfill | 0.0762 | 0.6 | 127 | [30] |
| Solder Bump + Underfill | 0.021–0.045** | 1.24–2.57 | 16.94–17.51 | This work |
| | 0.0762 | 2.6 | 29.31 | [30] |
| | 0.1 | 1.24 | 80.65 | [31] |
| | 0.102 | 0.8 | 127.5 | [32] |
| Substrate | 1 | 2 | 500 | [30] |
| Solder Ball + Air gap | 0.45 | 0.34 | 1323.53 | [30] |
| PCB | 1.6 | 0.3 | 5333.33 | [31] |

* The 2 μm of TEOS/SiN passivation layer [10] is assumed to be 1 μm thick per layer.
** The thickness of the solder bumps/underfill layer is assumed to be 0.6×$W_B$ [30].

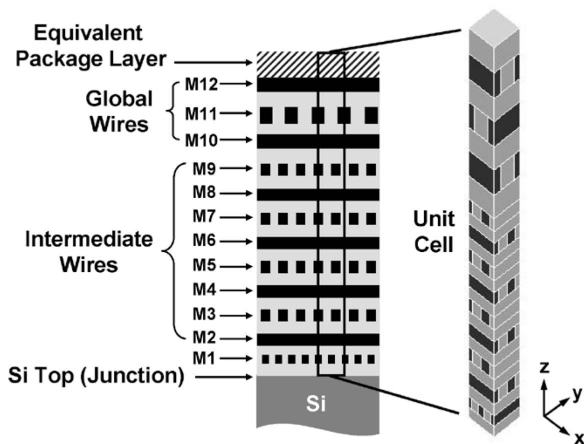


Fig. 7. FEM simulation geometry (unit cell) representing the periodic multilevel interconnect structure (45-nm technology node example).

orthogonal multilevel interconnects. The FEM simulator solves the 3-D heat diffusion equation under the steady-state

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} + \frac{q(T)}{K} = 0$$

where $q(T)$ is the temperature-dependent heat generation per unit volume (W/m$^3$) and $K$ is the thermal conductivity of the material. For the interconnects $q(T) = J_{\mathrm{rms}}^2 \rho(T)$ and for the other materials $q(T) = 0$, where $J_{\mathrm{rms}}$ is the rms current density and $\rho(T)$ is the temperature-dependent metal resistivity.

The spacing for M1 is assumed to be the same as the width of M1. The spacings for intermediate and global wires are slightly adjusted with the spacing to width ratio of 1–1.22. With adjusted spacings, the ratio of the number of M1, intermediate and global lines per unit area is found to be 4:3:2 for all technology nodes. Assuming that all metal lines are uniformly spaced with this ratio and infinitely long, a unit cell can be defined by symmetry planes as shown in Fig. 7. FEM simulations are performed for this unit cell, where four side walls satisfy symmetric (adiabatic) boundary conditions. The ITRS specified junction temperature $(T_j)$ and ambient temperature $(T_{\mathrm{amb}} = 45\ ^\circ\mathrm{C})$ are applied at the bottom of the unit cell and at the top of the equivalent package layer, respectively.

The metal-level- and technology-dependent rms current $(I_{\mathrm{rms}})$ values are applied to all wires as input loads in the

TABLE II
METAL-LEVEL- AND TECHNOLOGY-DEPENDENT DUTY RATIOS

| Tech. Node | 90 nm | 65 nm | 45 nm | 32 nm | 22 nm |
|---|---|---|---|---|---|
| Local | 0.016 | 0.034 | 0.040 | 0.041 | 0.044 |
| Intermediate | 0.132 | 0.158 | 0.175 | 0.182 | 0.180 |
| Global (logic) | 0.144 | 0.194 | 0.213 | 0.212 | 0.222 |
| Global (clock) | 0.287 | 0.387 | 0.427 | 0.424 | 0.445 |

electrothermal FEM simulations because interconnect Joule heating is determined by the rms current (or rms current density) as proved in Appendix I. The ITRS provides a single value of the maximum current density $(J_{\max})$ for intermediate wires at each technology node. First, we assume that the ITRS specified $J_{\max}$ is the average current density $(J_{\mathrm{avg}})$ and then calculate the average current $(I_{\mathrm{avg}})$ at each technology node by $I_{\mathrm{avg}} = J_{\mathrm{avg}} \times A_i$, where $A_i$ is the cross sectional area of intermediate wires. Assuming that $I_{\mathrm{avg}}$ is constant for all metal wires at a given technology node, the $I_{\mathrm{rms}}$ values are calculated by $I_{\mathrm{rms}} = I_{\mathrm{avg}}/r^{0.5}$, where $r$ is the metal-level- and technology-dependent duty ratio. In this paper, the duty ratios at different metal levels and technology nodes are calculated for the first time by using SPICE simulations (Table II). It must be noted that the methodology used for the duty ratio calculation follows the same principle as that used for predicting the clock frequencies and minimum logic depths in the ITRS. The detailed methodology and assumptions are described in Appendix II. In our FEM simulations, all model dimensions, material properties, and current loads are based on the ITRS data for high performance MPUs (Table III) and incorporated as parameters in the FEM code.

## IV. RESULTS AND DISCUSSION

Temperature contours within the orthogonal multilevel interconnects are obtained from fully coupled 3-D electrothermal FEM simulations. Each simulation is composed of two different cases depending on the duty ratio of global wires: 1) all global wires carry clock signals and 2) all global wires carry logic signals. In practical circuit environments, global wires can be used for both clock and logic signal transmissions. Therefore, the simulation results for these two cases can be regarded as two bounds of the predicted interconnect temperature. Fig. 8 plots the spatial chip temperature distributions along the vertical distance from the Si junction $(z = 0)$ to the topmost global wires for the case with clock global wires. For 90- and 65-nm nodes, the temperature rises within the interconnect stacks are less than 13 and 33 °C, respectively. However, metal temperatures increase significantly beyond 45-nm node owing to the combined effects of increasing metal resistivity, increasing current density, increasing number of global metal levels, and decreasing ILD thermal conductivity. The maximum metal temperature $(T_{\max})$ occurs at the topmost global wires as indicated in the contour plot. The maximum metal temperature rise with respect to the junction temperature $(\Delta T_{\max} = T_{\max} - T_j)$ is obtained for each simulation and used in the following thermal scaling analysis. Note that the total thickness of the $(\mathrm{Cu} + \mathrm{ILD})$ layers decreases with scaling, due to the smaller vertical dimensions of wires and insulators despite increasing number of metal levels. For the case with logic global wires, the shape of temperature profile

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TABLE III
ITRS-BASED SIMULATION PARAMETERS

| | | Technology Node (nm) | | | | |
|---|---|---|---|---|---|---|
| | | 90 | 65 | 45 | 32 | 22 |
| Wire Width (nm) | M1 | 107 | 76 | 54 | 38 | 27 |
| | Intermediate | 137.5 | 97.5 | 67.5 | 47.5 | 32.5 |
| | Global | 205 | 145 | 102.5 | 70 | 50 |
| Wire Height (nm) | M1 | 181.9 | 129.2 | 97.2 | 72.2 | 54 |
| | Intermediate | 233.75 | 175.5 | 121.5 | 90.25 | 65 |
| | Global | 430.5 | 319 | 235.75 | 168 | 125 |
| Wire Spacing* (nm) | M1 | 107 | 76 | 54 | 38 | 27 |
| | Intermediate | 147.83 | 105.17 | 76.5 | 53.83 | 39.5 |
| | Global | 223 | 159 | 113.5 | 82 | 58 |
| ILD Thickness (nm) | M1** | 181.9 | 129.2 | 97.2 | 72.2 | 54 |
| | Intermediate | 206.25 | 156 | 108 | 80.75 | 58.5 |
| | Global | 389.5 | 290 | 215.25 | 154 | 115 |
| Number of Metal Levels*** | Total | 10 | 11 | 12 | 12 | 14 |
| | M1 | 1 | 1 | 1 | 1 | 1 |
| | Intermediate | 7 | 8 | 8 | 8 | 8 |
| | Global | 2 | 2 | 3 | 3 | 5 |
| $\rho(T_j)$* (μΩ-cm) | M1 | 3.26 | 3.50 | 3.88 | 4.44 | 5.19 |
| | Intermediate | 3.08 | 3.24 | 3.57 | 4.00 | 4.66 |
| | Global | 2.88 | 2.97 | 3.15 | 3.44 | 3.81 |
| Thermal Conductivity* ($Wm^{-1}K^{-1}$) | $K_{ILD}$, $K_{IMD}$ | 0.40 | 0.30 | 0.21 | 0.16 | 0.12 |
| | $K_{ILD,eff}$ (min) | 0.44 | 0.34 | 0.25 | 0.20 | 0.16 |
| | $K_{ILD,eff}$ (max) | 10.66 | 10.56 | 10.80 | 10.70 | 11.03 |
| | $K_{U,eff}$ | 2.57 | 1.86 | 1.70 | 1.58 | 1.41 |
| Barrier Layer Thickness (nm) | | 10 | 7 | 5 | 3.5 | 2.5 |
| $k_{ILD}$ (bulk) | | 2.7 | 2.4 | 2.1 | 1.9 | 1.7 |
| $J_{max}$ ($MA/cm^2$) | | 0.5 | 1.0 | 3.0 | 4.3 | 5.8 |
| $I_{avg}$ (mA)* | | 0.161 | 0.171 | 0.246 | 0.184 | 0.122 |
| $T_j$ (°C) | | 90 | 85 | 85 | 85 | 85 |
| $T_{amb}$ (°C) | | 45 | 45 | 45 | 45 | 45 |
| $A_c$ ($mm^2$) | | 310 | 310 | 310 | 310 | 310 |
| Solder Bump Pitch (μm) | | 150 | 120 | 100 | 90 | 80 |
| Solder Bump Size (μm) | | 75 | 60 | 50 | 45 | 40 |
| Number of Solder Bumps**** | | 3072 | 3072 | 3840 | 4224 | 4416 |
| $R_{th,eq}$ ($mm^2K/W$)* | | 7175.54 | 7177.38 | 7175.67 | 7175.11 | 7175.05 |

* Calculated from this work using ITRS data.
** The ILD thickness for M1 (PMD thickness) is assumed to be the same as the height of M1.
*** The maximum numbers for intermediate and global tiers are 8 and 5, respectively.
**** The number of chip I/Os (number of total chip pads) for MPU.

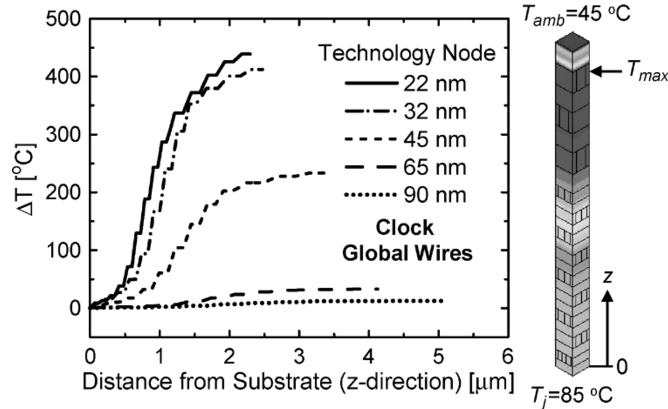


Fig. 8. Temperature rise with respect to the junction temperature ($\Delta T = T - T_j$) along the vertical distance from the Si junction (along the $z$ direction) for the case with clock global wires. The temperature contour plot of 45-nm technology node is also shown as an example. The metal-level- and technology-dependent duty ratios are used.

is similar but the absolute temperature rise is much higher, due to smaller duty ratios (hence larger $I_{\rm rms}$ values) and more Joule heating: $\Delta T_{\max} = 15\ °C-906\ °C$ (from 90- to 22-nm node).

Previous thermal simulations are often based on temperature-independent simulations using constant $\rho$ values at an arbitrary temperature (room temperature or junction temperature). Although temperature-dependent simulations using $\rho(T)$ generally require more computation times, errors induced by temperature-independent simulations must be carefully investigated.

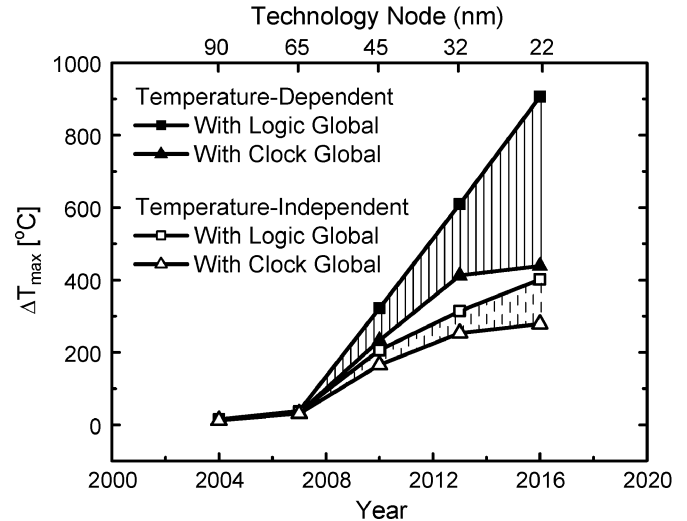


Fig. 9. Impact of temperature-dependent and temperature-independent simulations on $\Delta T_{\max}$. For temperature-independent simulations, constant $\rho$ values at $T_j$ are used. The size effect of $\rho$ is included for both cases and other simulation parameters are the same.

Fig. 9 compares the predictions for $\Delta T_{\max}$ from these two simulation methodologies, both of which include two cases with clock and logic global wires. As pointed out earlier, the case with clock global wires provides a lower bound of $\Delta T_{\max}$ and that with logic global wires, an upper bound of $\Delta T_{\max}$. Up to 65-nm node, the temperature-dependent and -independent simulations yield almost the same results with errors less than 2 °C. However, beyond 45-nm node, significant underestimations of $\Delta T_{\max}$ can be made by temperature-independent simulations. The temperature-dependent electrothermal simulation is shown to be necessary for accurate estimates of multilevel interconnect temperatures under aggressive thermal conditions. Furthermore, the predicted temperature range bounded by the upper and lower limits is shown to increase rapidly with scaling for the temperature-dependent simulations, which indicates that $\Delta T_{\max}$ will become more sensitive to the relative fraction of logic and clock global wires in advanced technology nodes.

The contribution of various factors to the total effective resistivity has been shown in Section II-A. The contribution of these resistivity components to $\Delta T_{\max}$ is compared in Fig. 10. Average $\Delta T_{\max}$ values are plotted based on two cases with clock and logic global wires. The average $\Delta T_{\max}$ considering all resistivity components ($\sim$ 670 °C) is much higher than that considering only bulk resistivity ($\sim$ 300 °C). If one or more resistivity components are neglected, $\Delta T_{\max}$ can be significantly underestimated especially in sub-50 nm technologies. Note that the impact of barrier layers on the average $\Delta T_{\max}$ is approximately the same as that of the other factors, contrary to its smallest contribution to the total resistivity (Fig. 1). The reason is that the reduced conductor cross section, by considering barrier layer, not only increases resistivity but also generates more Joule heating for a given current. The contribution of surface and grain boundary scattering to $\Delta T_{\max}$ is observed to be equally important, similar to their contributions to the total resistivity.

Next, we examine the impact of ILD thermal conductivity scaling on $\Delta T_{\max}$. Fig. 11 shows that if the ILD thermal conductivity is not properly scaled in accordance with the

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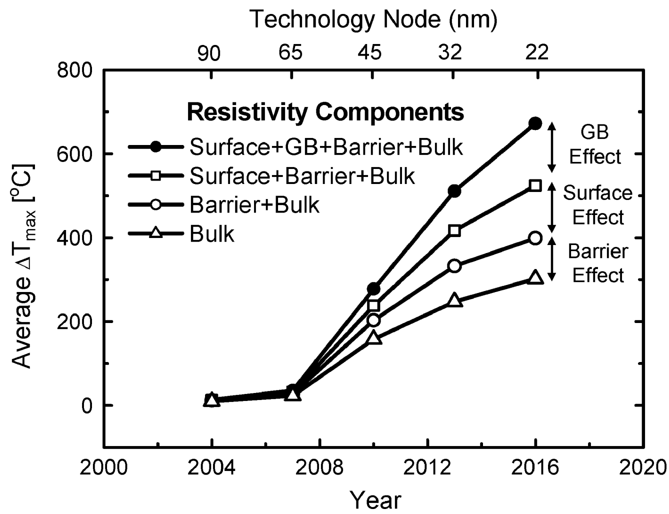


Fig. 10. Impact of resistivity scaling on average $\Delta T_{\max}$. Note that the temperature dependence of resistivity is still considered for all cases. All other parameters are scaled with technology. GB stands for grain boundary.

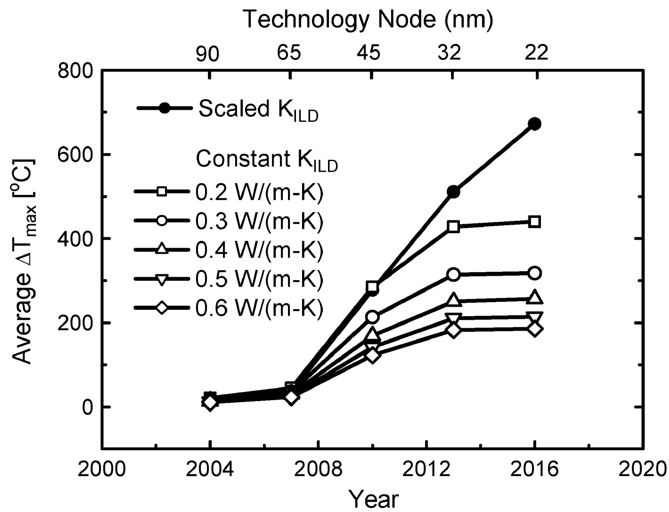


Fig. 11. Impact of ILD thermal conductivity scaling on average $\Delta T_{\max}$. Note that the fully scaled temperature- and size-dependent resistivity values are used here. All other parameters are scaled with technology.

decreasing dielectric constant, $\Delta T_{\max}$ can be significantly underestimated. Alternatively, this plot conveys a message that if $K_{\rm ILD}$ can be maintained constant at 0.6 W/(m-K), average $\Delta T_{\max}$ less than 200 °C can be achieved without violating other scaling rules.

Critical parameters affecting interconnect temperatures are metal resistivity, current density, and ILD thermal conductivity. So far we have followed the ITRS-provided design rule of maximum current density $(J_{\max})$, which is based on scaling of device and interconnect parameters (chip frequency, gate capacitance, gate width, fanout, wire capacitance, supply voltage, etc.). However, currently manufacturable solutions are not known for $J_{\max} > 2.5$ MA/cm$^2$ and for $k_{\rm ILD} < 2.4$ that approximately corresponds to $K_{\rm ILD} < 0.3$ W/(m-K). In order to provide thermal design guidelines, the contour lines of the average $\Delta T_{\max}$ are plotted in the $J_{\rm avg} - K_{\rm ILD}$ parameter space in Fig. 12. For lower $K_{\rm ILD}$ values, the average $\Delta T_{\max}$ increases more rapidly with $J_{\rm avg}$ indicated by the closer spacing between

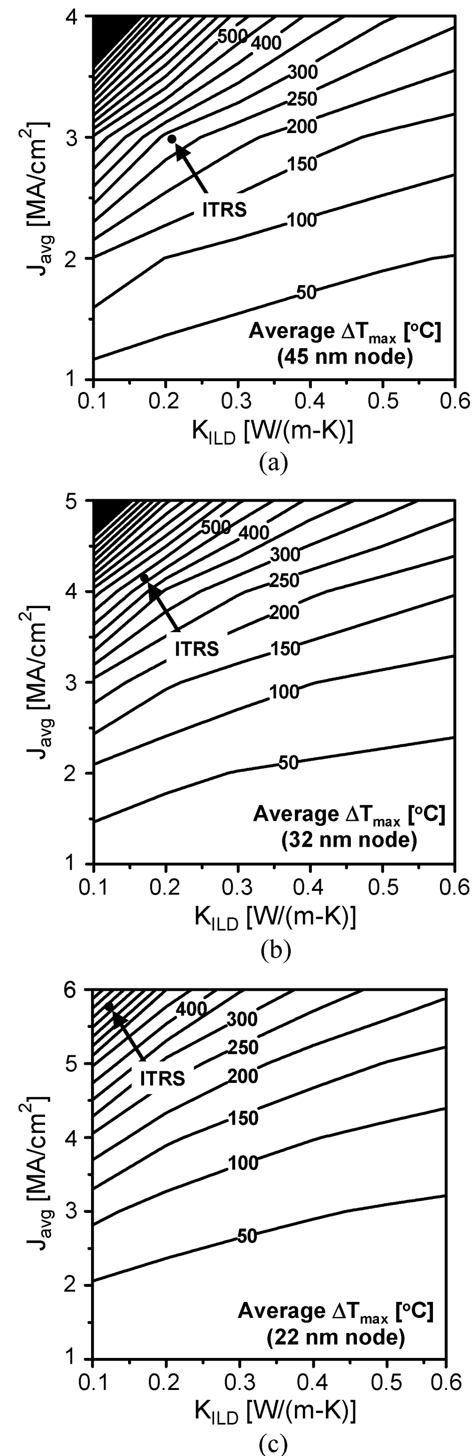


Fig. 12. Contour lines of the average $\Delta T_{\max}$ in the $J_{\rm avg} - K_{\rm ILD}$ parameter space for (a) 45-nm node, (b) 32-nm node, and (c) 22-nm node. The contour lines denote average $\Delta T_{\max}$ values from two cases with clock and logic global wires, increasing in steps of 50 °C. The shaded regions in (a) and (b) indicate temperature rises above the melting point of Cu $(\Delta T_{\max} > 1000$ °C). The ITRS requirements for $J_{\rm avg}$ and $K_{\rm ILD}$ are also indicated.

isotherms. Moving toward the higher $K_{\rm ILD}$ values will provide more room for the current density design. Note that for the same $J_{\rm avg} - K_{\rm ILD}$ pair, the average $\Delta T_{\max}$ continuously decreases from 45 to 22 nm node due to increasing duty ratios (decreasing rms current and Joule heating). A proper choice of

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$J_{\mathrm{avg}} - K_{\mathrm{ILD}}$ parameter sets can achieve reasonably low metal temperatures while still preserving other scaling trends.

## V. Conclusion

A rigorous scaling analysis of multilevel interconnect temperatures in high performance ICs has been performed using 3-D electrothermal FEM simulations. Detailed calculations of Cu resistivity have considered various scattering mechanisms, barrier layer effect, and temperature dependence. A methodology for extracting the correlation between thermal conductivity and dielectric constant of low-$\kappa$ materials has been presented based on fully physical models. In addition, an accurate thermal model has been proposed to account for the thermal impact of vias. The comprehensive scaling analysis based on fully coupled technological, structural and material factors has showed that the average maximum interconnect temperature rise is expected to be about 300–700 °C in sub-50-nm interconnect technologies. It has been shown that the interconnect Joule heating problem will become more severe due to coupled effects of increasing metal resistivity, increasing current density, and decreasing ILD thermal conductivity if other variables follow the ITRS scaling rules. Although increasing metal resistivity might be an inevitable consequence of wire dimension scaling, it could be alleviated by reducing barrier layer/Cu interface roughness (increasing $p$) and by reducing the grain boundary density and impurity enrichment (decreasing $R$). Minimizing barrier layer thickness can also be an object of further investigation. Developing nonporous low-$\kappa$ dielectric materials with higher thermal conductivity and considering optimal density thermal vias during the early design phase might be other solutions to enhance heat dissipation and achieve lower interconnect temperatures.

## Appendix I

This section provides a simple proof of why interconnect Joule heating is determined by the rms current. The rms (or the effective) value of any time-varying current (or voltage) is defined as the square root of the mean value of the squared function. For example, for a periodic current function

$$I(t) = I_0 \cos(\omega t + \phi) \tag{AI1}$$

the rms value of the current is given by

$$I_{\mathrm{rms}} = \sqrt{\frac{1}{T}\int_{t_0}^{t_0+T} I^2(t)dt} = \sqrt{\frac{1}{T}\int_{t_0}^{t_0+T} I_0^2 \cos^2(\omega t + \phi)dt} \tag{AI2}$$

where the mean value of the current is obtained by integrating $I^2(t)$ over one time period, (i.e., from $t_0$ to $t_0 + T$), and then dividing by the range of integration, $T$.

Now consider that a periodic current (shown in (AI1)) flows along an interconnect of resistance $R$. The average power dissipated due to Joule heating is the average of the instantaneous power $(p)$ over one period $(= T)$, which can be expressed as

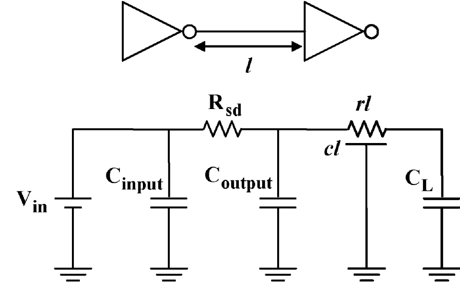


Fig. 13. Equivalent circuit diagram for an inverter driving an interconnect and a load.

$$P_{\mathrm{avg}}^{\mathrm{int}} = \frac{1}{T}\int_{t_0}^{t_0+T} p\,dt = R\frac{1}{T}\int_{t_0}^{t_0+T} I_0^2 \cos^2(\omega t + \phi)dt. \tag{AI3}$$

Comparing (AI2) and (AI3) reveals that the average power dissipated in the interconnect of resistance $R$ is simply the product of the rms value of the current and $R$

$$P_{\mathrm{avg}}^{\mathrm{int}} = I_{\mathrm{rms}}^2 R. \tag{AI4}$$

## Appendix II

This section describes the strategy used to evaluate typical values of duty ratio at different interconnect metal levels (local, intermediate, and global) and at different technology nodes. The duty ratio for a metal interconnection is the ratio of the time (per clock cycle) when it carries a current to the clock time period. The duty ratio is determined by various factors such as the current drive strength, the dimensions of the wire and the effective capacitive loading on the signal being driven. In this work, the typical VLSI circuit scenario of a gate driving an appropriate interconnection and a capacitive load is used to estimate the metal duty ratio by using SPICE simulations. Without any loss of generality, the driver and load are chosen to be inverter gates of appropriate sizes and fanout. The circuit and its equivalent representation for such a configuration are shown in Fig. 13.

The driver gate is represented by a voltage source and an equivalent resistance $R_{\mathrm{sd}}$ which corresponds to its parasitic source/drain resistance as well as the input gate capacitance. The load driven by this gate is composed of the output parasitic capacitance (junction/diffusion capacitance plus gate-overlap capacitance) of the driving gate, the $R-C$ network corresponding to the interconnection and the total input gate capacitances of the gates being driven. The relevant device/gate driver parameters are used in this work, based on ITRS predictions. The ITRS provides gate and overlap capacitances ($C_{\mathrm{gn}}$ and $C_{\mathrm{ovn}}$, respectively) for a typical NMOS device. The corresponding figures for a minimum sized inverter are calculated by assuming a PMOS-NMOS sizing ratio of 2 (to roughly match PMOS/NMOS drive currents). Hence, the gate input capacitance is calculated as

$$C_{\mathrm{input}} = C_{\mathrm{gn}} + C_{\mathrm{gp}} = 3 \cdot C_{\mathrm{gn}}. \tag{AII1}$$

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In calculating the parasitic output capacitance for a minimum-sized inverter, the junction capacitance of a gate is assumed to be half of its input capacitance [33]. The gate output capacitance is given by

$$C_{\mathrm{output}} = (C_{\mathrm{jn}} + C_{\mathrm{jp}}) + (C_{\mathrm{ovn}} + C_{\mathrm{ovp}}) = \left(\frac{3}{2}C_{\mathrm{gn}}\right) + (3 \cdot C_{\mathrm{ovn}}). \quad \text{(AII2)}$$

The gate overlap capacitance includes the worst-case Miller effect which causes an increase in the effective capacitance.

Local wires have the smallest cross section dimensions with high resistance (and capacitance) per unit length and are used for providing the interconnections between nearby gates and devices so that the length is not too long. Since these wires carry signals over short distances, the wire delay is not very high and the drivers for these signals are usually minimum sized gates so as to give minimum switching delay and hence best performance for the logic circuitry. Since local interconnections are mostly used for logic circuitry, the load capacitance is calculated assuming that it drives a fanout of four, as done in the familiar FO4 delay calculations. The typical local interconnection length is assumed to be $9\lambda$, where $\lambda$ is the layout parameter, one half of the minimum feature size for a particular technology node. The effective resistivity for Cu considers the size-dependent surface and grain boundary scatterings at $T_j$. Capacitance values are extracted using FastCap [34].

In the case of intermediate and global wires, the wire lengths are much longer and minimum sized drivers are not enough to drive the large loads while meeting the timing requirements. Buffers (repeaters in the form of inverters) need to efficiently drive signals over the long interconnections. These buffers have sizes much larger than the minimum sized gates. Increasing driver sizes improves their drive current, but also increases the load capacitance and hence the sizes and interbuffer separation is optimized so as to achieve minimum delay. The commonly used optimal delay buffer insertion methodology [35] is used to find appropriate driver sizes and interconnection lengths for global wires. The optimal delay interbuffer distance is found to be of the same order as the maximum interconnect length over which delay is equal to the *RC* delay of the interconnect $(\tau = RC)$ [1]. For intermediate level interconnections, the wire length is assumed to be the same as the $\tau = RC$ length as provided by ITRS, while driver and load sizes are determined by the same procedure as for global interconnections. Unlike local wires, global and intermediate wires do not drive a fanout of four. Instead, the load is the input capacitance of the next buffer stage which is of the same size as the driver itself. For global interconnections, it is a good rule of thumb to assume the rise time of the input signal to the driver as 10% of the clock period [36]. This assumption has been applied for both intermediate and global wires in these simulations.

Other assumptions used for all these calculations are as follows. The on-time for each metal interconnection is taken as the time for which it carries a current greater than 10% of the maximum current value, for each cycle. One transition per clock cycle is assumed, which is a typical behavior for wires carrying logic signals. In the case of global wires, however, which are most often used for chip-wide communication of signals such as the clock which obviously undergo two transitions per clock cycle, two values of duty ratio are shown—one assuming a single transition and the other assuming two transitions per clock cycle.

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