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Temperature-Dependent Thermal Conductivity of Undoped Polycrystalline Silicon Layers[1]

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Polycrystalline silicon is used in microelectronic and microelectromechanical devices for which thermal design is important. This work measures the in-plane thermal conductivities of free-standing undoped polycrystalline layers between 20 and 300 K. The layers have a thickness of 1 μm, and the measurements are performed using steady-state Joule heating and electrical-resistance thermometry in patterned aluminum microbridges. The layer thermal conductivities are found to depend strongly on the details of the deposition process through the grain size distribution, which is investigated using atomic force microscopy and transmission electron microscopy. The room-temperature thermal conductivity of as-grown polycrystalline silicon is found to be 13.8 $W \cdot m^{-1} \cdot K^{-1}$ and that of amorphous recrystallized polycrystalline silicon is 22 $W \cdot m^{-1} \cdot K^{-1}$, which is almost an order of magnitude less than that of single-crystal silicon. The maximum thermal conductivities of both samples occur at higher temperatures than in pure single-crystalline silicon layers of the same thickness. The data are interpreted using the approximate solution to the Boltzmann transport equation in the relaxation time approximation together with Matthiessen's rule. These measurements contribute to the understanding of the relative importance of phonon scattering on grain and layer boundaries in polysilicon films and provide data relevant for the design of micromachined structures.

KEY WORDS: grain boundary scattering; polycrystalline silicon; phonon scattering; thermal conductivity.

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1. INTRODUCTION

Polycrystalline silicon (polysilicon) is used in many microelectronic and microelectromechanical (MEMS) devices [1]. Examples include the gate layer in a CMOS transistor, thin film transistors (TFT) in static random access memories and active matrix liquid crystal displays, and micromachined thermal actuators. In these applications, different deposition conditions are used to address specific performance targets or processing requirements. While CMOS uses as-grown polysilicon layers, TFTs use amorphous silicon recrystallized to form polysilicon and MEMS devices use low-stress polysilicon layers. Because the performance and reliability of many of these devices are influenced by heat conduction [2], the thermal conductivities of their constituent polysilicon layers need to be determined.

The thermal conductivity of single-crystal silicon layers of thickness between 0.1 and 1.6 μm have been measured at temperatures between 20 and 300 K [3–5]. In contrast to single-crystal silicon, polysilicon consists of many individual grains. The grain boundaries scatter phonons, the energy quanta of lattice vibrations, which reduces the thermal conductivity. The thermal properties of polysilicon cannot be inferred from single-crystal silicon data due to the variability of grain sizes. Depending on the growth and annealing conditions, the grain size and structure can vary, yielding different physical properties [6]. Electrical transport cannot be used to probe the effect of grains since measurements on polysilicon are complicated by the dopant distribution. Therefore, thermal transport studies are ideal to probe grain size and distributions. A few researchers have studied polysilicon [7–12], but these data encompass a very small temperature range, near room-temperature only. The room-temperature thermal conductivity of undoped polysilicon layers has been reported to be in the range 15 to 25 $W \cdot m^{-1} \cdot K^{-1}$ [11] and that of doped silicon to be in the range 17 to 34 $W \cdot m^{-1} \cdot K^{-1}$ [7–10, 12]. Measurements down to 100 K have been performed on a few of the doped polysilicon samples [12]. However, many of the important parameters including the deposition temperature, film thickness, average grain size, and dopant type and concentration were not given. The doped samples are not ideally suited for probing the effect of grains since, in addition to phonon grain boundary scattering, the phonon electron and phonon impurity scattering complicates the results. Therefore, it is important to perform thermal conductivity measurements of undoped layers, and low-temperature data, which are not available in the literature, are particularly useful since they amplify the impact of grain boundary scattering.

The present work investigates the effects of grain structure on the thermal conductivities of undoped polysilicon layers of thickness near 1 μm at

temperatures between 30 and 300 K using Joule heating and electrical-resistance thermometry in a microfabricated structure. The approximate solution to the Boltzmann transport equation in the relaxation time approximation is used together with Matthiessen's rule to provide fundamental information about phonon scattering. The results are useful for the thermal design of microelectronic and microelectromechanical devices that use polycrystalline silicon layers.

2. EXPERIMENTAL METHODS

2.1. Growth and Characterization

Polycrystalline silicon layers were grown using low-pressure chemical vapor deposition (LPCVD) in a Tylan furnace with a silane (SiH_4) flow of 136 sscm, a hydrogen flow of 110 sccm, and a process pressure of 400

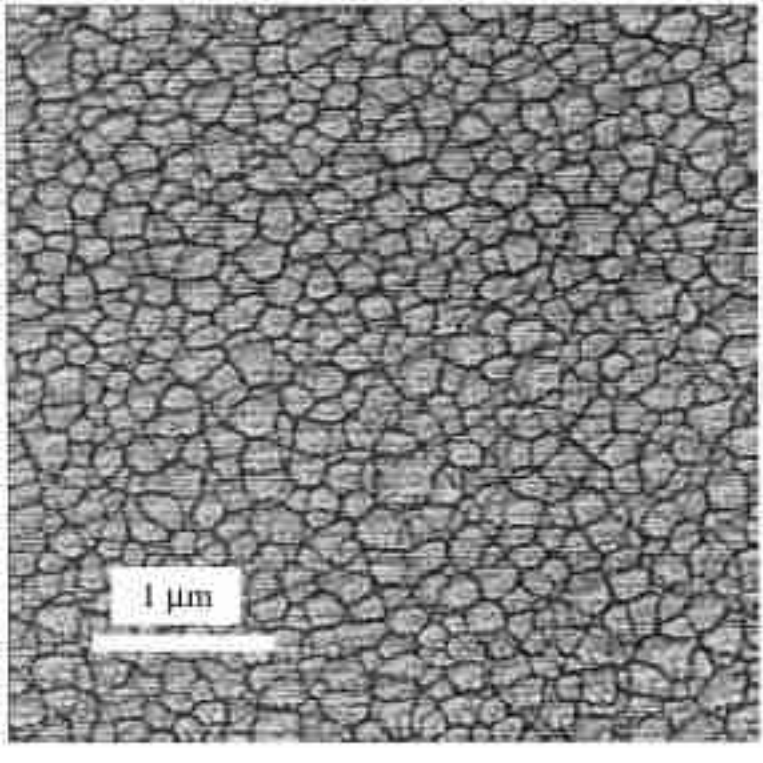

Fig. 1. Plan-view AFM image of polysilicon sample A showing the grains. The average grain size extracted using this image is 210 nm.

mTorr. One sample (sample A) was grown at a temperature of 620°C, and another sample (sample B) was grown at a temperature of 525°C and annealed at 900°C for 1 h. While sample A is an as-grown polysilicon, sample B is amorphous recrystallized polysilicon, which yields a different microstructure. Atomic force microscopy (AFM) and transmission electron microscopy (TEM) images were used to determine the average grain size using the line-intercept method. A Digital Instruments Nanoscope Dimension 3000 atomic force microscope was used to obtain the plan-view image (Fig. 1) of sample A. The polysilicon grain size obtained from the plan view is estimated to be 210 ± 28 nm. In the case of sample B, it was necessary to use transmission electron microscopy since the surface roughness is very small. The polysilicon grain size obtained from the plan view TEM of sample B is estimated to be 190 ± 10 nm (Fig. 2). However, the cross-sectional TEM reveals a different microstructure for the two cases. Sample A has a nonhomogeneous grain structure, whereas sample B has a random

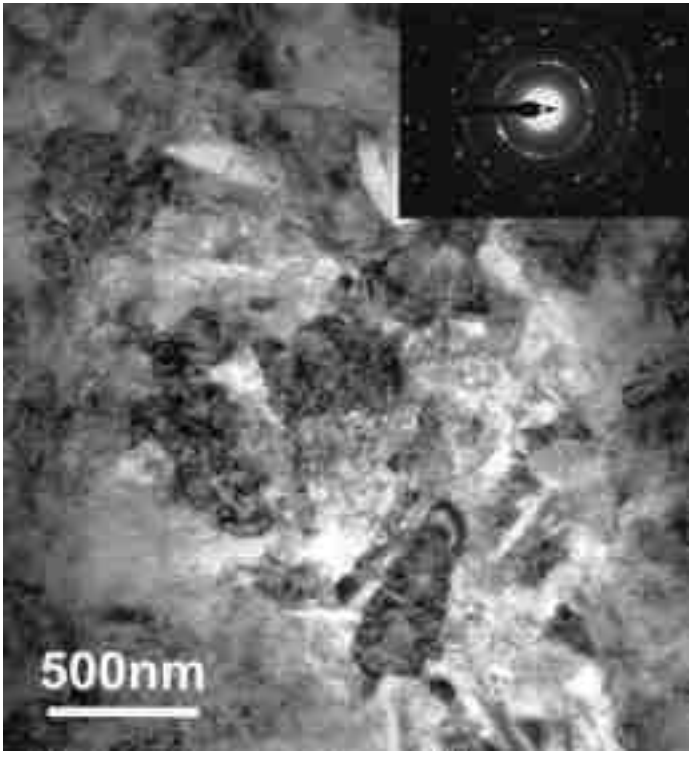

Fig. 2. Plan-view TEM image of polysilicon of sample B showing the grains. The grain size is 190 nm.

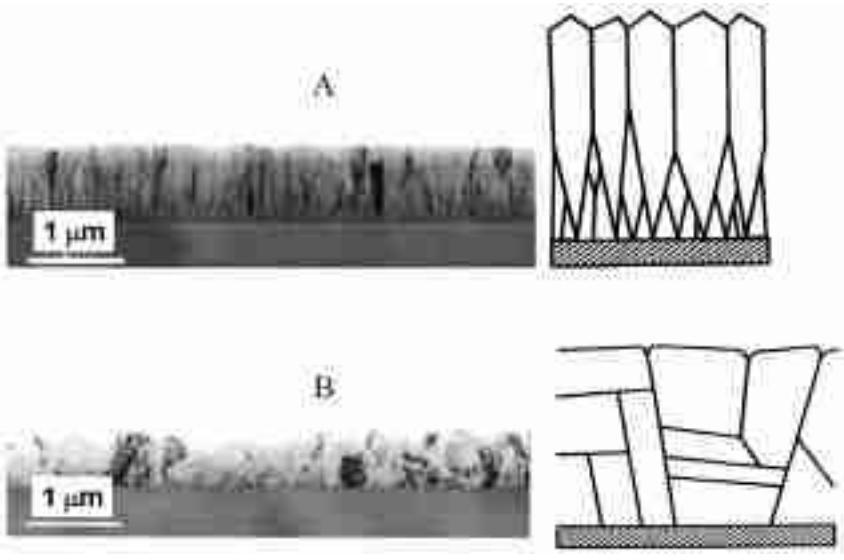

Fig. 3. Grain structure of polysilicon layers observed using cross-sectional TEM: (A) Non-homogeneous structure of sample A. (B) Random structure of sample B.

grain structure as shown in Fig. 3, which is anticipated due to the different growth process [1, 6]. Many of the crystallites in sample A resemble a cone, with smaller nucleation points near the oxide substrate growing larger toward the top surface of the polycrystalline silicon layer. This means that the grain size measured from a plan-view sample from the near-surface part of the film would have a larger average value than the grain size at the near-substrate part.

2.2. Thermal Conductivity Measurement Technique

Figure 4 shows the structure used for lateral thermal conductivity measurements, which are performed in vacuum using steady-state Joule heating and electrical-resistance thermometry in patterned aluminum microbridges [13, 14]. The aluminum bridges are patterned using lithography and chemical wet etching, and the free-standing structure is fabricated using deep reactive ion etching with a deposited silicon dioxide layer as the etch stop. The polyimide layer protects the aluminum bridges against chemical corrosion during processing and provides mechanical strength for the free-standing layer. The structure dimensions and materials are chosen carefully to ensure that the temperature rise in the sensor is dominated by the thermal resistance for lateral conduction in the polysilicon layer. Three

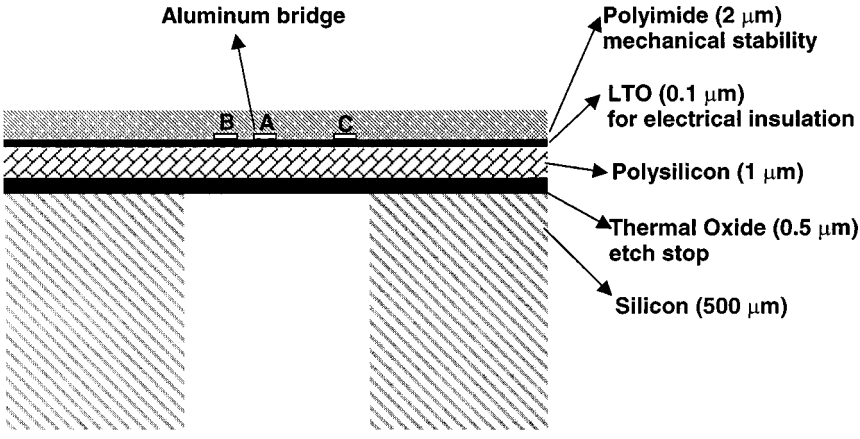

Fig. 4. Experimental structure used to measure the thermal conductivity of polysilicon (not to scale).

aluminum bridges with width 1 μm and thickness 0.2 μm serve as the two resistive temperature detectors (RTD) and the heater. The nonlinearity in the current–voltage (I–V) characteristics of the aluminum bridges results from Joule heating and is used to determine suitable currents for the heater bridge and the sensors, in which Joule heating must be negligible. Bridge A is used as a heater, and bridges B and C are used to determine temperature change due to Joule heating. The lateral thermal conductivity is determined using a simple solution to the one-dimensional heat conduction equation,

$$k = \frac{(Q/2)\,\Delta X}{S(T_B - T_C)} \tag{1}$$

where Q is the heater power dissipated in a length ($L = 1$ mm) of the heater bridge, ΔX is the distance between B and C, $S = d \times L$ is the cross-sectional area for heat conduction, where d is the thickness of the polysilicon layer (1 μm), and T_B and T_C are the temperatures at B and C, respectively. The measurements are performed in the temperature range 20 to 300 K using a Lakeshore MTD-135 continuous-flow cryostat. A diode sensor with an accuracy of 0.5 K in the temperature range 10 to 100 K and 1% in the temperature range 100 to 300 K is used for the temperature control. The fraction of heat lost through radiation is always less than 8% over the entire temperature range and less than 2% below 150 K. The fraction of heat conducted by the silicon dioxide and polymer layers, which are used for mechanical support and protection, is always less than 1% over the temperature range of the study. The experimental uncertainty in the thermal

conductivity is less than 14%. The main contribution arises from the uncertainties in the structure dimensions, in particular, the structure geometry.

3. THERMAL CONDUCTIVITY MODELING

The temperature dependence of the thermal conductivity of crystalline solids is governed by the temperature dependence of the phonon specific heat and the rates of phonon scattering on other phonons, impurities, defects, charge carriers, boundaries, and dislocations [15–19]. While phonon–phonon scattering is the chief mechanism contributing to room-temperature thermal resistance, phonon-boundary scattering limits the mean free path of the phonons at lower temperatures. The phonon grain-boundary scattering depends on the grain size and structure and is therefore calculated in a different manner for sample A and sample B.

3.1. Impact of a Random Grain Structure

To calculate the thermal conductivity of the random grain polycrystalline silicon as in sample B, the approximate solution to the Boltzmann transport equation in the relaxation time approximation has been used. According to the model developed by Callaway [15] and refined by Holland [18], the thermal conductivity is

$$k = \tfrac{1}{3} v^2 \int_0^{\theta_D/T} c_v \tau \, dx_\omega \tag{2}$$

Here θ_D is the Debye temperature, v is the velocity of the phonons, and τ is the relaxation time. The dimensionless frequency is given as $x_\omega = \hbar\omega/(k_B T)$, where ω is the phonon angular frequency, $\hbar$ is Planck's constant divided by 2π, T is the temperature, and k_B is the Boltzmann constant. Reductions in the relaxation time due to an umklapp process (τ_u), phonon defect scattering (τ_{defect}), and phonon grain-boundary scattering (τ_{grain}) have been taken into account [4, 19] using Mathiessen's rule.

$$\frac{1}{\tau} = \frac{1}{\tau_u} + \frac{1}{\tau_{defect}} + \frac{1}{\tau_{grain}} \tag{3}$$

The expressions for the scattering rate τ_u and τ_{defect} are taken from the literature [18]. The grain-boundary scattering rate (τ_{grain}) is calculated in a manner similar to that of Graebner et al. [20, 21] using the expression

$$\tau_{grain}^{-1} = \frac{v}{d}\left(\frac{1-p(\omega)}{1+p(\omega)}\right) \tag{4}$$

$p(\omega)$ is the probability of specular reflection, and d is the average grain dimension obtained from the plan view, which is 190 nm in the case of sample B.

3.2. Impact of a Nonhomogeneous Grain Structure

Ideally the grain structure of a polysilicon thin film deposited above 620°C is expected to be columnar. However, in most layers the grain structure is found to be nonhomogeneous [6] and quite similar to the microstructure of CVD diamond [20–26]. In a typical nonhomogeneous grain structure of polysilicon like sample A, the grain sizes are found to increase from the bottom of the layer to the top, so a linear approximation can be used to describe the grain size.

$$d(z) = (d_{\max} - d_{\min}) \frac{z}{d_L} + d_{\min} \tag{5}$$

Here z is the coordinate perpendicular to the layer; $d(z)$ is the grain size perpendicular to the layer; $d_{\min}$ is the minimum grain size, which occurs at the bottom of the layer; $d_{\max}$ is the maximum grain size, which occurs at the top of the layer (210 nm for sample A); and d_L is the film thickness. The increase in the average grain size from the bottom of the layer to the top leads to a corresponding increase in the mean free path and relaxation time. The average heat flux $q_a(x_\omega)$ along the layer can be determined using

$$q_a(x_\omega) = -\frac{c_v v^2}{3 d_L} \left(\frac{dT}{dx_\omega} \right) \int_0^{d_L} \tau(z)\, dz \tag{6}$$

Here x is the coordinate along the layer. The lateral thermal conductivity is given by

$$k = -\left(\frac{dT}{dx} \right)^{-1} \int_0^{\theta_D/T} q_a(x_\omega)\, dx_\omega \tag{7}$$

This expression is valid for a nonhomogeneous grain structure as long as the phonon mean free path is much shorter than the film thickness. When the thickness of the film becomes comparable to the mean free path, the Boltzmann transport equation must be solved for a more accurate representation of the thermal conductivity [23]. The room-temperature mean free path of single-crystalline silicon layers has been reported to be 300 nm [5] and that of polysilicon, which depends on the grain size and structure, is less than 75 nm. The reduction in the mean free path in polysilicon is caused largely by the presence of intragrain defects. Since the mean free

path is much smaller than the thickness of the layer, the present model is a reasonable approximation, especially to investigate the lateral thermal conductivity. However, the present model may underestimate the impact of grain-boundary scattering at low temperatures.

4. RESULTS AND DISCUSSION

Figure 5 presents experimental data for the room-temperature thermal conductivity of undoped polysilicon layers as a function of the deposition temperature. The thermal conductivity of sample A at room temperature (298 K) is 13.8 $W \cdot m^{-1} \cdot K^{-1}$ and that of sample B is 22 $W \cdot m^{-1} \cdot K^{-1}$, which is an order of magnitude less than the thermal conductivity of a single-crystal silicon layer of the same thickness at room temperature. This result compares well with the room temperature thermal conductivity value of 15 to 23 $W \cdot m^{-1} \cdot K^{-1}$ of undoped polysilicon reported in the literature [11]. The high-temperature annealing has caused an improvement in the

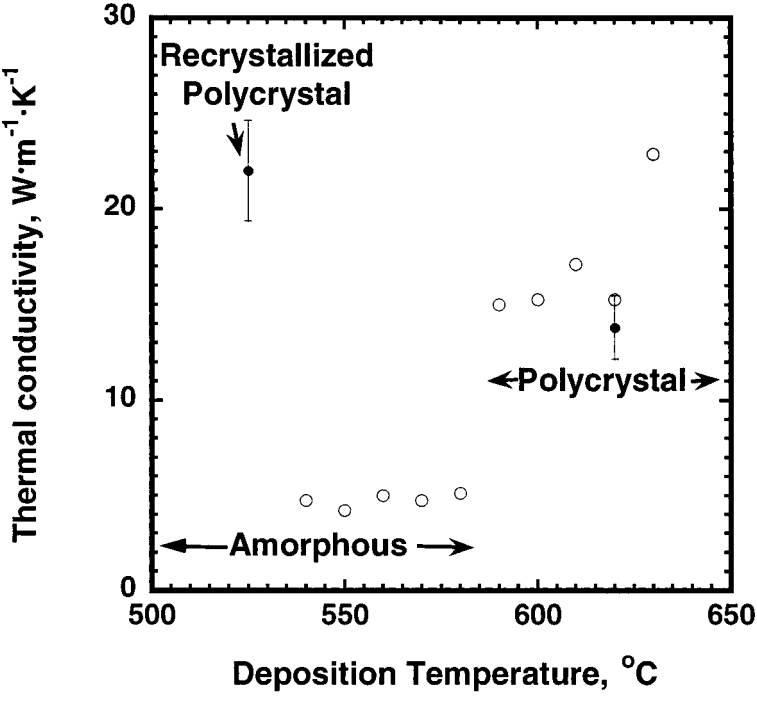

Fig. 5. Room-temperature thermal conductivity of polysilicon layers: (●) present work; (○) Wei et al. [11].

thermal conductivity of sample B compared to sample A. In fact the room-temperature thermal conductivity of amorphous silicon deposited around 525°C is $5\ W \cdot m^{-1} \cdot K^{-1}$ [11] and improves to $22\ W \cdot m^{-1} \cdot K^{-1}$ due to the high-temperature anneal. It should be mentioned that phosphorus and boron doping of the layers are usually accompanied by a high-temperature anneal, which increases the grain size and therefore the thermal conductivity. This may explain the higher thermal conductivities reported in the literature for doped polysilicon [12]. Figure 6 presents the low-temperature thermal conductivity data for undoped polysilicon layers and other forms of silicon to illustrate the impact of the polysilicon grains. The maximum values of the thermal conductivity are $14.5\ W \cdot m^{-1} \cdot K^{-1}$ for sample A and $32.6\ W \cdot m^{-1} \cdot K^{-1}$ for sample B, which occur at temperatures of 156 and 256 K, respectively. The maximum thermal conductivity value in a thin layer of single-crystal silicon is reduced by an order of magnitude compared to that in bulk single-crystal silicon due to phonon

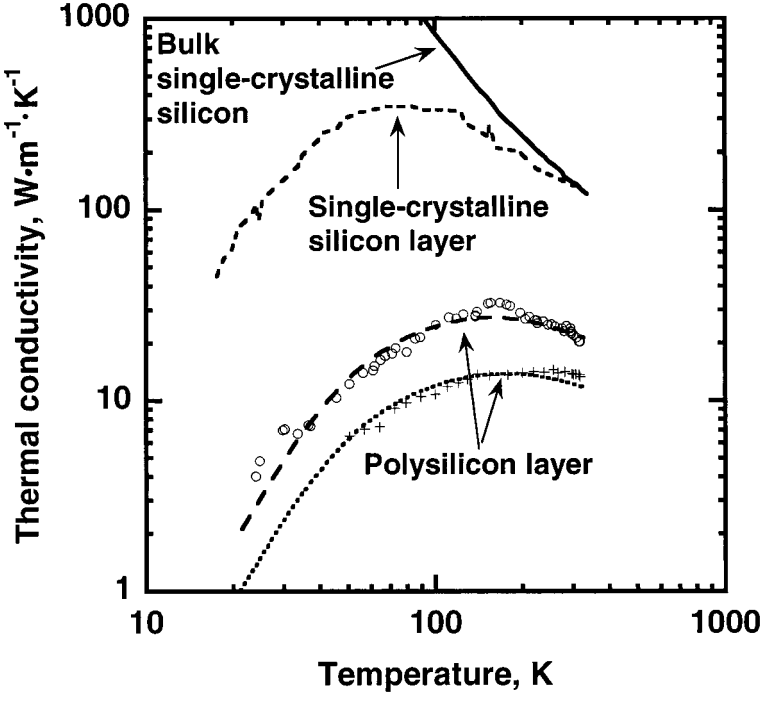

Fig. 6. Thermal conductivity of polysilicon layers in the temperature range 30 to 300 K. (+) Sample A experiment; (○) sample B experiment. Dotted line, sample A theoretical model; long-dashed line, sample B theoretical model; short-dashed line, single-crystalline silicon layer; solid line, bulk silicon.

scattering on the layer boundaries. Phonon scattering on grain boundaries results in a further order-of-magnitude reduction in thermal conductivity for a polysilicon layer compared to a single-crystal layer.

The model described in the previous section provides a reasonably good fit to the experimental data as illustrated in Fig. 6. In the case of sample B, the only fitting parameter is the point defect scattering. In addition to defect scattering, $d_{\min}$ is also a fitting parameter in sample A, for which a value of 10 nm was used. In both the samples, umklapp scattering is similar to that in the case of single-crystalline silicon thin films, and grain-boundary scattering is dependent on the average grain size. Diffuse scattering, which occurs when the surface is rough on the scale of the phonon wavelength, has been taken into account.

It is important to note that it is not a trivial task to obtain information regarding the defect density. While techniques like high-resolution TEM can provide this information, it is always likely that the defects were incorporated during the sample preparation. In addition, TEM is performed on only a small region of the sample, so determining an average defect density using this method may not be accurate. In this regard, temperature-dependent transport studies are useful to probe the defects. The relaxation time for phonon defect scattering is given by $\tau_{\text{defect}} = (A\omega^4)^{-1}$, where A is a constant that is directly proportional to the defect density and the mass difference introduced by the defect. The constant A is found to be $1.33 \times 10^{-43}\,\text{s}^3$ for sample A and $6.932 \times 10^{-44}\,\text{s}^3$ for sample B, and the point defect density is calculated to be $1.815 \times 10^{19}\,\text{cm}^{-3}$ and $9.417 \times 10^{18}\,\text{cm}^{-3}$ for the two samples, respectively. The value of A reflects the increase in the number of defects in polysilicon compared to single-crystalline silicon [4], which is anticipated. In addition to the imperfections existing in single-crystal sample, *viz*., dislocations, stacking faults, etc., polysilicon also has in-grain microtwins and dangling bonds, which affect the transport properties. Another interesting point is that the defect scattering is stronger in the case of sample A compared to sample B, and the reason could be the high-temperature anneal, which reduces the in-grain defects. It might be important to consider additional scattering mechanisms due to extended defects, dislocations, and stacking faults to develop a more accurate model. Also, grains as large as 500 nm are present in the sample, so using an average grain size is an approximation. This may also add to the deviation of the model from the experimental data.

5. SUMMARY AND CONCLUSIONS

This work measures the temperature-dependent thermal conductivities of polysilicon layers with varying grain structures. This study also shows

the advantage of high-temperature annealing in lowering the effective lateral thermal resistance and yields transport models that can be incorporated into simulations of practical semiconducting devices, which are of particular relevance for those subjected to electrical overstress.

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