Short-Timescale Thermal Mapping of Semiconductor Devices

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***Abstract*—We report spatial mapping of temperature fields in semiconductor devices with sub-microsecond temporal resolution. The measurements are performed at a facility that integrates scanning laser-reflectance thermometry with electrical stressing capability. Data for SOI LDMOS transistors investigate transient heat diffusion within the buried silicon dioxide and capture large temperature gradients in the drift region, which result from the spatially-varying impurity concentration. The new thermometry facility is promising for the study of transistor and interconnect thermal failure due to electrostatic discharge (ESD).**

I. Introduction

SEMICONDUCTOR devices must withstand short-timescale electrical stressing phenomena, some of which induce severe degradation or failure due to the resulting temperature rise. Electrostatic discharge (ESD), for example, can yield device or interconnect melting during current pulses shorter than 100 ns [1], [2]. Transistors can be designed to better withstand such stressing through thermal design, which relies on accurate simulation capability. But simulation of thermal failure phenomena need transient temperature-field data for verification and improvement of model parameters. Recent research developed techniques for mapping steady-state temperature fields in semiconductor devices [3]–[7], but the technically critical problem of transient thermometry has not received much attention. Transient thermometry of SOI LDMOS transistors was performed by Arnold *et al.* [8], who used the temperature-dependent bias current to investigate transistor cooling after heating pulses of duration comparable to 1 μs. This method has the advantage that it does not require any modification of devices. But this approach does not yield the spatial variation of temperature within a device. This letter communicates thermal mapping of SOI LDMOS transistors with high temporal and spatial resolution using laser-reflectance thermometry, which detects temperature changes near a surface using the temperature-dependence of optical properties [9]–[13].

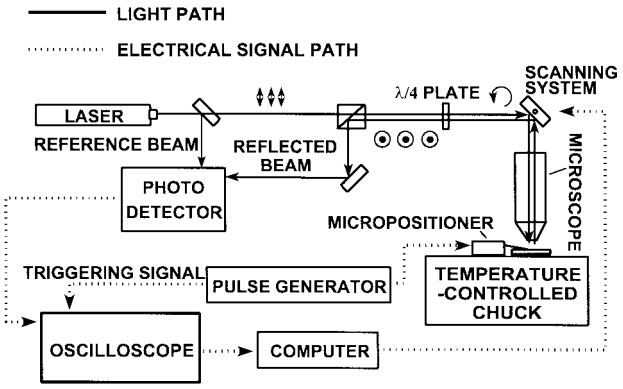

Fig. 1. Facility for scanning laser-reflectance thermometry. Galvanometrically-actuated scanning mirrors for the probe laser allow short-timescale thermal mapping without motion of the sample or the micropositioners.

II. Experiments

Measurements are performed at the facility shown in Fig. 1, which integrates scanning laser diagnostics and electrical probing. Radiation from a laser diode is coupled into an optical microscope and focused to a diameter near the wavelength, 820 nm. A polarization cube and a quarter-wave plate separate the incident and reflected probe beam paths. The radiation powers are captured using photodiodes with 500 MHz bandwidth and a digital oscilloscope with 1 GHz sampling frequency. Laser power fluctuations are subtracted using a reference beam drawn by a beam splitter. The probe laser focus is scanned over the wafer surface using a pair of galvanometrically-actuated mirrors that rotate about orthogonal axes, while the semiconductor device remains stationary.

The technique is applied to SOI LDMOS transistors fabricated using BESOI substrates and the method of Leung *et al.* [7]. The drift region is 40 μm long and the total device area, including the enclosed drain, is 0.32 mm^2. The total width of the drift region is 2 mm. To assist with the thermometry, an aluminum layer of thickness 25 nm is sputtered within the surface oxide as shown in Fig. 2. Because the aluminum layer is opaque to radiation at 820 nm, it prevents interaction between the radiation and the transistor and precisely defines the vertical location at which temperature is measured. But

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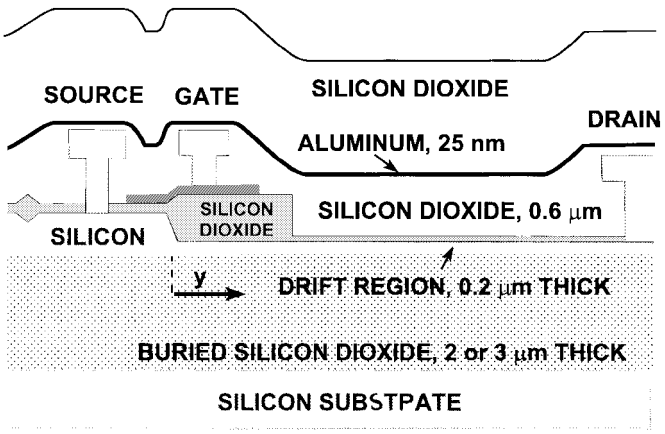

Fig. 2. Cross-sectional view of the SOI LDMOS transistor used in the present thermometry study. The surface silicon dioxide contains a 25-nm aluminum layer, which prevents radiation interaction with the transistor and sharply defines the vertical position of the temperature measurement.

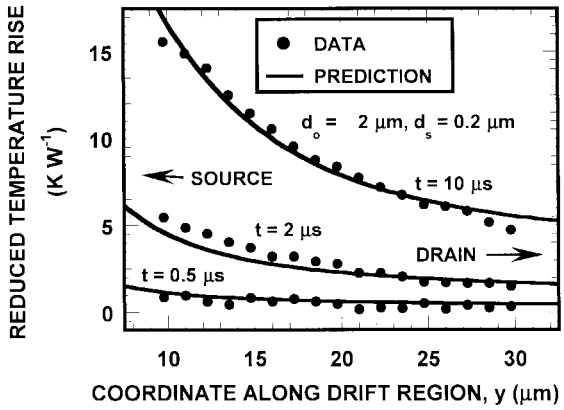

Fig. 3. Temperature distribution above the drift region of an SOI LDMOS transistor for varying values of the time after the pulse initiation. Also shown are predictions based on the linear impurity-concentration distribution in the drain region, which is targeted by the transistor fabrication process.

the presence of the aluminum and its separation from the drift region limits the spatial and temporal resolution of the measurements. To reduce the total thickness of the silicon dioxide layer, part of the thermal oxide, shown as a gray region on top of the drift region in Fig. 2, is etched away before the deposition of a CVD oxide layer. The importance of lateral heat conduction within the aluminum layer can be estimated by using the thermal decay length [14], $L_D = (k_a d_a d_o/k_o)^{1/2}$, where k_a and d_a are the aluminum thermal conductivity and thickness, respectively, and k_o and d_o are the thermal conductivity and thickness of the oxide separating the aluminum from the device. The thermal decay length is $\sim$1 μm, resulting in a spatial resolution limit that is important but not more restrictive than that due to the diffraction of the incident probe laser beam. The spatial resolution limit due to heat spreading within the silicon dioxide layer is comparable to its thickness, 0.6 μm, and is also not more restrictive than that due to the diffraction. The temporal resolution limit due to the silicon dioxide is approximately given by the time required for heat to diffuse normal to the layer, $t_D = L_{ox}^2/\alpha_o$, where L_{ox} is the thickness of the oxide layer and α_o is the thermal diffusivity of silicon dioxide. The thermal diffusion time is around 0.5 μs for the LDMOS transistors studied here.

Periodic voltage pulses of duration near 30 μs and magnitude near 30 V are applied to the drain with a duty cycle less than 0.01. The gate of the power LDMOS transistor is positively biased at 12 V and the source is grounded. The probe laser beam remains at each location long enough to average the transient photodetector signals during a thousand heating periods. The spatial temperature-rise map at any time is extracted from the periodic temperature-rise data at each point. The temperature dependence of the surface reflectance is calibrated in the absence of electrical heating using a thermal chuck. The relative uncertainty in the absolute magnitude of temperature rise is 20%, which mainly comes from the calibration of the thermoreflectance coefficient. But the uncertainty in the ratio of the temperature rises at any locations or times, which is important for the temporal and spatial shapes of the temperature field, is less than 5%. The noise equivalent temperature resolution is about 0.1 K.

III. Results and Discussion

Fig. 3 shows the temperature distribution measured along the drift region of an SOI LDMOS transistor for varying times after the initiation of the heating pulse. Since the thermal diffusion time normal to the *buried* silicon dioxide is comparable to 5 μs, the data actually describe transient heat diffusion within the silicon dioxide surrounding the active region. The temperature rise increases with decreasing coordinate y due to the spatial variation of the phosphorus impurity concentration. A linear increase in the impurity concentration with coordinate y is targeted by the fabrication process of the LDMOS transistors to improve their voltage-blocking capability [7]. Since the current density does not vary significantly within the drift region, the rate of heat generation is proportional to the local electrical resistivity. The electrical resistivity decreases with increasing impurity concentration, and therefore the volumetric heating rate decreases with increasing y.

Fig. 3 also shows the predictions of a finite-difference solution to the transient, two-dimensional heat equation in the drift region and surrounding silicon dioxide. The simulation uses bulk resistivity data for phosphorus-doped silicon with concentration distribution that is consistent with the fabrication process. The thermal conductivity and heat capacity used for the calculations are 100 W m^{-1} K^{-1} and 1.66×10^6 J m^{-3} K^{-1} for silicon and 1.4 W m^{-1} K^{-1} and 1.65×10^6 J m^{-3} K^{-1} for silicon dioxide, respectively [15]. The simulation assumes that the top boundary condition for the passivation is adiabatic and the bottom boundary condition for the buried silicon dioxide is isothermal. These assumptions are justified by the extremely low convection and radiation heat losses to the ambient air [5] and by the short timescale of the heating pulse, respectively. The shape and time dependence of the calculated temperature rise agree well with the data.

The spatially averaged temperature rise per unit power per unit area of the drift region in the plane of the substrate is

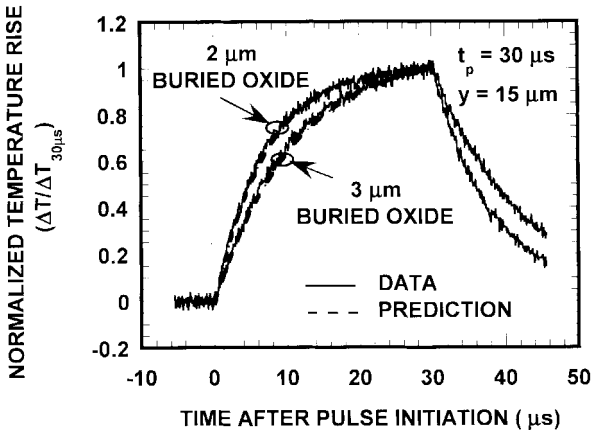

Fig. 4. Comparison of the transient temperature-rise shape at a single location above the drift region of LDMOS transistors with two different buried silicon-dioxide thicknesses. To facilitate shape comparison, the data and predictions are normalized by their values at 30 μs.

8×10^{-7} K m^2 W^{-1} at the time 10 μs after the initiation of the pulse. While this differs from the similarly normalized transient thermometry data of Arnold *et al*. [8], we have shown theoretically that this difference can be almost entirely explained by the difference in the interrogated domain and the dimensions of the devices. Remaining differences may be due to the fact that Arnold *et al*. [8] measured a weighted average of the temperature in the drift region.

Fig. 4 compares the shapes of the transient temperature rises measured using laser-reflectance thermometry for two values of the buried silicon-dioxide thickness. To make the differences in shape as clear as possible, the temperature-rise curves are normalized by their values at 30 μs. The time for heat to diffuse to the nearly-isothermal substrate increases with the thickness of the buried silicon dioxide. This causes the shape of the temperature rise for the case of the 2-μm buried silicon dioxide to flatten more rapidly than that for the case of the 3-μm buried silicon dioxide. This difference in shape agrees well with the predictions of the numerical solutions to the transient one-dimensional heat equation, also shown in the figure, which are hard to distinguish from the experimental data.

IV. Conclusions

The temperature distributions along the drift region of SOI LDMOS transistors are measured using a laser thermoreflectance technique. The nonhomogeneity of the impurity concentration in the drift region yields a steep increase in temperature near the source. The scanning laser-reflectance technique described here achieves better temporal resolution when the radiation interacts with the region whose temperature is to be detected. This has been shown by subsequent work, which has demonstrated temporal resolution of 10 ns for interconnects on polymer passivation layers [16]. This resolution is promising for future failure studies during electrical overstress phenomena such as electrostatic discharge.

References

[1] A. Amerasekra and J. Verwey, "ESD in integrated circuits," *Qual. Reliab. Eng. Int.*, vol. 8, pp. 259–272, 1992.
[2] M. Chan, S. S. Yuen, Z.-J. Ma, K. Hui, P. K. Ko, and C. Hu, "Comparison of ESD protection capability of SOI and bulk CMOS output buffers," in *Proc. IEEE Int. Reliab. Phys. Symp.*, San Jose, CA, Apr. 11–14, 1994, pp. 292–298.
[3] R. Ostermeier, K. Brunner, G. Abstreiter, and W. Weber, "Temperature distribution in Si-MOSFET's studied by micro Raman spectroscopy," *IEEE Trans. Electron Devices*, vol. 39, pp. 858–863, 1992.
[4] R. J. T. Bunyan, M. J. Uren, J. C. Alderman, and W. Eccleston, "Use of noise thermometry to study the effects of self-heating in submicrometer SOI MOSFET's," *IEEE Electron Device Lett.*, vol. 13, pp. 279–281, 1992.
[5] K. E. Goodson, M. I. Flik, L. T. Su, and D. A. Antoniadis, "Prediction and measurement of temperature fields in silicon-on-insulator electronic circuits," *ASME J. Heat Transfer*, vol. 117, pp. 574–581, 1995.
[6] A. Majumdar, J. P. Carrejo, and J. Lai, "Thermal imaging using the atomic force microscope," *Appl. Phys. Lett.*, vol. 62, pp. 2501–2503, 1993.
[7] Y. K. Leung, Y. Suzuki, K. E. Goodson, and S. S. Wong, "Self-heating effect in lateral DMOS on SOI," in *7th Int. Symp. Power Semiconductor Devices and IC's*, Yokohama, Japan, May 23–25, 1995, pp. 136–140.
[8] E. Arnold, H. Pein, and S. P. Herko, "Comparison of self-heating effects in bulk-silicon and SOI high-voltage devices," in *IEDM Tech. Dig.*, 1994, pp. 813–816.
[9] E. Welsch, M. Reichling, C. Gobel, D. Schafer, and E. Matthias, "Modulated thermoreflectance imaging of hidden electric current distributions in thin-film layered structures," *Appl. Phys. Lett.*, vol. 61, pp. 916–918, 1992.
[10] W. Claeys, F. Giroux, S. Dilhaire, C. Gounelle, V. Quintard, and P. Mortini, "Temperature measurements on metallic lines under current stress by laser probing and correlation with electromigration tests at wafer level," *Multilevel Interconnection, SPIE*, vol. 2090, pp. 197–202, 1993.
[11] C. P. Grigoropoulos, A. A. Rostami, X. Xu, S. L. Taylor, and H. K. Park, "Transient reflectivity measurements and heat transfer modeling in laser annealing of semiconductor films," *Int. J. Heat Mass Transfer*, vol. 36, pp. 1219–1229, 1993.
[12] P. W. Epperlein, "Micro-temperature measurements on semiconductor laser mirrors by reflectance modulation: A newly developed technique for laser characterization," *Jpn. J. Appl. Phys.*, vol. 32, no. 12A, pp. 5514–5522, 1993.
[13] K. E. Goodson, O. W. Käding, M. Rösler, and R. Zachai, "Experimental investigation of thermal conduction normal to diamond-silicon boundaries," *J. Appl. Phys.*, vol. 77, no. 4, pp. 1385–1392, 1995.
[14] C. G. Shirley, "Steady-state temperature profiles in narrow thin-film conductors," *J. Appl. Phys.*, vol. 57, no. 3, pp. 777–784, 1985.
[15] K. E. Goodson, Y. S. Ju, M. Asheghi, O. W. Käding, M. N. Touzelbaev, Y. K. Leung, and S. S. Wong, "Microscale thermal characterization of high-power silicon-on-insulator transistors," (and references therein) in *Proc. 31st ASME National Heat Transfer Conf.*, Houston, TX, Aug. 1996, vol. 5, pp. 1–9.
[16] Y. S. Ju and K. E. Goodson, "Short-timescale thermal mapping of interconnects," presented at *Int. Reliab. Phys. Symp.*, Denver, CO, April 7–10, 1997.