# Enhanced phonon scattering by nanovoids in high thermoelectric power factor polysilicon thin films

Marc T. Dunham, Bruno Lorenzi, Sean C. Andrews, Aditya Sood, Mehdi Asheghi, Dario Narducci, and Kenneth E. Goodson

Citation: Appl. Phys. Lett. **109**, 253104 (2016); doi: 10.1063/1.4972483
View online: http://dx.doi.org/10.1063/1.4972483
View Table of Contents: http://aip.scitation.org/toc/apl/109/25
Published by the American Institute of Physics

# Enhanced phonon scattering by nanovoids in high thermoelectric power factor polysilicon thin films

Marc T. Dunham,[1] Bruno Lorenzi,[2] Sean C. Andrews,[3] Aditya Sood,[1,4] Mehdi Asheghi,[1] Dario Narducci,[2] and Kenneth E. Goodson[1]
[1]*Department of Mechanical Engineering, Stanford University, Stanford, California 94305, USA*
[2]*Department of Materials Science, University of Milano Bicocca, Milan, Italy*
[3]*Department of Chemical Engineering, Stanford University, Stanford, California 94305, USA*
[4]*Department of Materials Science and Engineering, Stanford University, Stanford, California 94305, USA*

(Received 15 September 2016; accepted 2 December 2016; published online 20 December 2016)

The ability to tune the thermal conductivity of semiconductor materials is of interest for thermoelectric applications, in particular, for doped silicon, which can be readily integrated in electronic microstructures and have a high thermoelectric power factor. Here, we examine the impact of nanovoids on the thermal conductivity of highly doped, high-power factor polysilicon thin films using time-domain thermoreflectance. Voids are formed through ion implantation and annealing, evolving from many small (~4 nm mean diameter) voids after 500 °C anneal to fewer, larger (~29 nm mean diameter) voids with a constant total volume fraction after staged thermal annealing to 1000 °C. The thermal conductivity is reduced to 65% of the non-implanted reference film conductivity after implantation and 500 °C anneal, increasing with anneal temperature until fully restored after 800 °C anneal. The void size distributions are determined experimentally using small-angle and wide-angle X-ray scattering. While we believe multiple physical mechanisms are at play, we are able to corroborate the positive correlation between measurements of thermal conductivity and void size with Monte Carlo calculations and a scattering probability based on Matthiessen's rule. The data suggest an opportunity for thermal conductivity suppression combined with the high power factor for increased material $zT$ and efficiency of nanostructured polysilicon as a thermoelectric material. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4972483]

The development of high-performance thermoelectric devices for both thermal management and thermal energy harvesting has been largely focused on increasing the dimensionless thermoelectric figure of merit, $zT = (S^2\sigma/k)*T$, with Seebeck coefficient $S$, electrical conductivity $\sigma$, and thermal conductivity $k$. Several materials are attractive for thermoelectric applications due to high $zT$ values near specific temperatures, for example, SiGe near 1000 K ($zT \sim 0.8$–$1.2$) and $Bi_2Te_3$ near room temperature ($zT \sim 1$).[1] The use of silicon as a thermoelectric material offers several benefits, including the wealth of processing knowledge within the semiconductor industry, elemental abundance, low toxicity, and lower cost, when compared with other materials that have seen widespread adoption in thermoelectric generators and Peltier coolers.[2] Bulk silicon has been regarded as a generally poor thermoelectric material due to its high thermal conductivity ($k \sim 140\ \mathrm{W\ m^{-1}\ K^{-1}}$),[3] which significantly reduces the figure of merit. However, precise nanostructuring has shown some success in reducing the thermal conductivity while preserving a desirable electrical conductivity because of the relative phonon and electron mean free paths in silicon. This is evident in recent results for silicon nanowires, which are engineered with dimensions that cause phonon energy carriers to scatter while minimizing additional scattering of electrons.[4,5] Silicon nanowires have been reported in the literature with thermal conductivities on the order of $1\ \mathrm{W\ m^{-1}\ K^{-1}}$, with $zT$ approaching 1.[4] However, the fabrication and reliability of silicon nanowires in devices remains challenging including the specific problem of maintaining electrical contact across the tips of bundles of nanowires.[6] Altering the phonon contribution to thermal conductivity is also possible by modifying the internal structure, where crystal grains and defects introduce scattering sites. Porous silicon structures are of particular interest as efficient phonon scatterers, and simulations[7] and measurements[8,9] have been reported in the literature for nanoscale to macroscale pores. Implantation of helium ions followed by thermal annealing is known to produce cavities or voids within silicon,[10–13] including highly boron-doped polycrystalline silicon for which an anomalous increase in the Seebeck coefficient and electrical conductivity has been observed due to a two-phase silicon-boride precipitate near the grain boundaries.[14–16] We report a reduction in thermal conductivity of highly doped polysilicon films, positively correlated with an evolving size distribution of nanoscale voids resulting from helium ion implantation. Experimental findings are supported by a Monte Carlo scattering model and scaling arguments.

Thin films of polycrystalline silicon are deposited to a thickness of 450 nm on a Si substrate with an 88 nm thermal $SiO_2$ dielectric barrier using chemical vapor deposition (CVD) at 600 °C. The films are boron-doped by ion implantation at 60 keV and $2.0 \times 10^{16}\ \mathrm{cm^{-2}}$ to a nominal concentration of $4.4 \times 10^{20}\ \mathrm{cm^{-3}}$, followed by 30 s of damage recovery at 1050 °C. Grains were found by TEM to be columnar, with dimensions of ~150 nm in the cross-plane and ~50–80 nm in the in-plane directions. A set of samples is implanted with He using a two-step implantation process at 90 keV with a fluence of $4 \times 10^{16}\ \mathrm{cm^{-2}}$, and 58 keV with a

fluence of $1.5 \times 10^{16}\,\mathrm{cm}^{-2}$, through a ~250 nm thick sacrificial aluminum layer. The aluminum layer is then removed with an HCl etch, and the films are subjected to a sequence of thermal annealing processes in an argon-heavy atmosphere. The first sample is annealed for 2 h at 500 °C, the second for 2 h at 500 °C followed by 2 h at 600 °C, and so on until the sixth annealed sample is processed at a high temperature of 1000 °C for a total of 6 annealing stages after helium implantation.[12] Samples undergoing thermal annealing are referenced by "T" followed by the highest anneal temperature (e.g., T500 for 500 °C max anneal).

Time domain thermoreflectance (TDTR), an optical pump-probe method, measures the cross-plane thermal conductivity of the thin film polysilicon samples. TDTR is a well-established technique, which is used to measure the thermal conductivity of thin films and bulk materials. Further details of our TDTR setup can be found in the literature along with extensive work from other groups on the application of this method for thermal transport studies.[17–22] An aluminum transducer layer is deposited on top of all polysilicon films and a thermally grown 50 nm $SiO_2$/Si witness sample simultaneously by electron-beam evaporation. The thickness of the transducer layer is determined using a Tencor Alpha-Step 500 Surface Profiler to be 56 nm. The pump beam is amplitude modulated at a frequency of 1 MHz and heats the sample through absorption within the Al transducer layer. The time delayed probe beam measures the temporal rate of decay of temperature at the surface of the sample by interrogating the reflectivity of the Al layer. In these measurements, the pump and probe beams are focused down to $1/e^2$ spot diameters of ~10 and 6 $\mu$m.[17] The total optical power incident onto the sample is limited to ~10 mW, resulting in a steady state temperature rise less than 2 K. The amplitude of the in-phase and out-of-phase voltage signals from the RF lock-in amplifier, correlated with surface temperature decay, is normalized at +100 ps and fit to a three-dimensional thermal model using a non-linear least squares routine to simultaneously extract the cross-plane thermal conductivity of polysilicon and the Al/poly-Si thermal boundary resistance (TBR). For the 56 nm aluminum transducer layer, we assume a heat capacity of 2.44 MJ $m^{-3}$ $K^{-1}$ and a thermal conductivity of 100 W $m^{-1}$ $K^{-1}$. For the poly-Si and Si substrate layers, we assume a heat capacity of 1.66 MJ $m^{-3}$ $K^{-1}$ and a substrate thermal conductivity of 148 W $m^{-1}$ $K^{-1}$. For the buried $SiO_2$ layer, we assume a heat capacity of 1.62 MJ $m^{-3}$ $K^{-1}$, a thermal conductivity of 1.38 W $m^{-1}$ $K^{-1}$, and a TBR of 5 $m^2$ K $GW^{-1}$ at the poly-Si/$SiO_2$ and $SiO_2$/Si interfaces, on the order of TBR values extracted by Käding *et al.*[23] A sensitivity plot for the significant parameters in the current study is provided in Fig. 1(a), generated by calculating the fractional change in normalized amplitude signal ($R$) per unit fractional perturbation in the parameter $X$, as $S_X = \delta\log(R)/\delta\log(X)$. The fitting parameters, $TBR_{\mathrm{Al/poly\text{-}Si}}$ and $k_{\mathrm{poly\text{-}Si}}$, are marked in bold font. For clarity, the sensitivities to poly-Si in-plane conductivity, aluminum conductivity, poly-Si/$SiO_2$ and $SiO_2$/Si TBRs, $SiO_2$ and Si (substrate) heat capacities, and poly-Si thickness are not shown as their maximum sensitivities are less than 0.04. Figure 1(b) shows data and best fits for two samples that have the lowest and highest conductivities of the poly-Si samples. As validation, a witness sample consisting of 50 nm thick thermally grown $SiO_2$ on silicon substrate was coated in the same aluminum evaporation step and fit to a thermal conductivity of 1.33 W $m^{-1}$ $K^{-1}$ in good agreement with the literature.[24] On the polysilicon samples, measurements are taken at three spots per sample. For 6 of 8 measured samples, the spatial variation in conductivity is less than 3%, while 2 samples in the set (T600 and T1000) show a maximum spatial variation of 11%. Error bars are calculated by combining in quadrature ±5% uncertainty in aluminum transducer thickness and standard deviation from 3 spot measurements per sample. The Al/poly-Si TBR for all our samples falls within the range of 7–9 $m^2$ K $GW^{-1}$, except for T1000 where TBR is ~12 $m^2$ K $GW^{-1}$. No systematic variation of TBR with final annealing temperature is observed.

The evolution of thermal conductivity as a function of processing condition in Fig. 2 shows that the films initially exhibit a 57% reduction in thermal conductivity after helium ion implantation (35% after the first thermal annealing step) but that the value returns to the level of the untreated sample after the high annealing temperature step reaches approximately 800 °C. A previous study of the Seebeck coefficient and electrical conductivity of identically prepared films demonstrated a significant jump in thermoelectric power factor due to a combination of effects including dopant reactivation and an energy filtering mechanism from the formation of

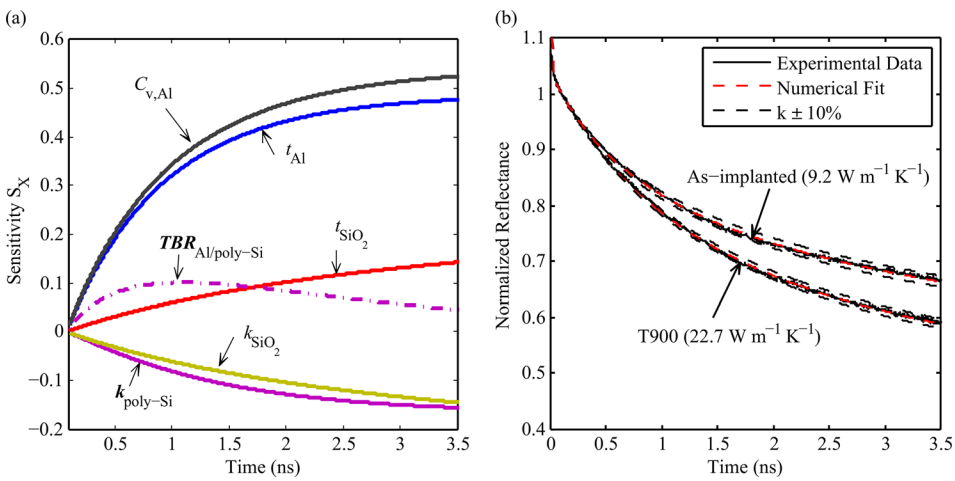


FIG. 1. (a) Plot of signal sensitivity to most significant system parameters and (b) fitting curves of normalized reflectance data for low (as-implanted) and high (T900) conductivity samples in the present study.

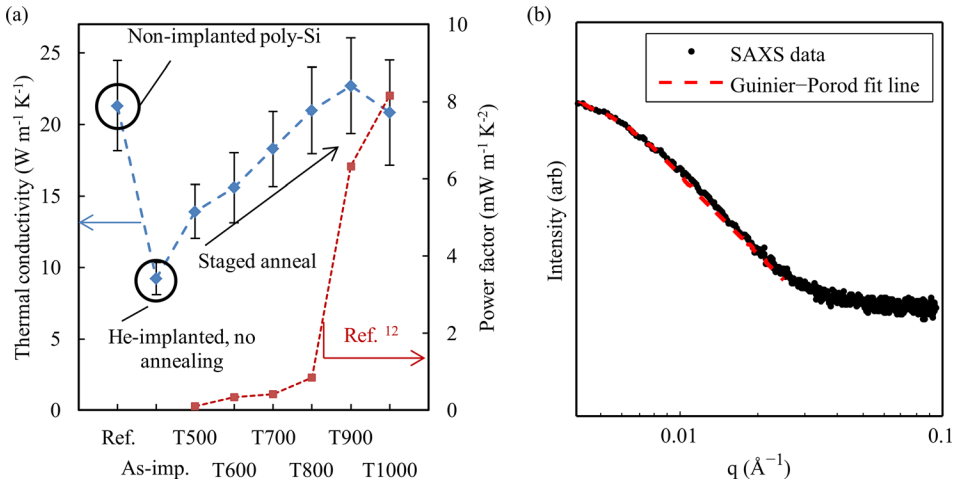


FIG. 2. Plot of (a) measured thermal conductivity (this work) and power factor[12] across the measured sample set and (b) representative SAXS data collected on a log-log scale for sample T800 with Guinier-Porod fit line.

silicon-boron precipitate at the grain boundaries,[12] but unfortunately not until the thermal conductivity was observed to have returned to non-implanted levels in this study, as shown in Fig. 2(a). It was considered that the reduction in thermal conductivity could be due at least in part to grain growth through the annealing process. Plan-view SEM images were prepared, and the average grain intercept method was applied to confirm no significant variation in lateral grain size through the annealing process. Previous cross-section TEM imaging on similar samples also indicated no grain growth through the conditions used in this study,[15] in agreement with previous studies showing the capability of boron to pin grain boundaries.[25]

Increases in electrical conductivity due to dopant reactivation (indicated by an initial rise in boron impurity concentration from Hall measurements) during thermal recovery from helium implantation will also contribute to an increased electronic thermal conductivity, which is calculated in Table I as $k_{\text{e,in-plane,WFL}}$ using the Wiedemann-Franz-Lorenz relation. While in-plane grains are known to be smaller than cross-plane grains in these samples, which indicates higher electron thermal conductivity in the cross-plane direction, expected anisotropy ratios (~2–3) still suggest less than 5% contribution to total thermal conductivity from electron transport. Wide-angle and small-angle X-ray scattering (WAXS/SAXS) data were obtained to quantitatively evaluate the mean diameter and size distribution of nanovoids through the range of film processing conditions. This technique has been previously utilized to characterize nano- and micro-scale void and defect structures in polysilicon.[26,27] A set of representative SAXS data recorded for the T800 sample, fit using the Guinier-Porod model, is given in Fig. 2(b).

We propose that the rise in measured thermal conductivity is due, at least in part, to the evolution of voids from many small voids to fewer larger voids reported from the X-ray measurements. To test this hypothesis, we begin with a simple Matthiessen's rule model considering phonon-boundary, phonon-phonon, and phonon-void scattering, and assuming a fixed, circular scattering cross-section using mean void diameter $D$

$$\frac{1}{\Lambda} = \frac{1}{\Lambda_{\text{p-b}}} + \frac{1}{\Lambda_{\text{p-p}}} + \frac{1}{\Lambda_{\text{p-v}}} = \frac{1}{\Lambda_{\text{p-b}}} + \frac{1}{\Lambda_{\text{p-p}}} + \frac{n\pi D^2}{4}. \quad (1)$$

For constant total void volume fraction $F$, with number density $n$ and single void volume $V$, $nV = F$, the expression for phonon mean free path becomes

$$\Lambda = \frac{1}{\frac{1}{\Lambda_{\text{p-b}}} + \frac{1}{\Lambda_{\text{p-p}}} + \frac{3F}{2D}}. \quad (2)$$

The phonon mean free path will increase with void diameter assuming constant total void volume fraction $F$ (assumed approximately 0.5% from previous studies[13]),

TABLE I. Experimental doping and transport data as a function of maximum annealing temperature.

| Sample label | $T_{\text{a,max}}$ (C) | $B_{\text{Si}}$ (cm$^{-3}$) | $\rho_{\text{in-plane}}$ (Ω m) | $k_{\text{e,in-plane,WFL}}$ (W m$^{-1}$ K$^{-1}$) | $d_{\text{void,avg}}$ (nm) | $k_{\text{poly-Si}}$ (W m$^{-1}$ K$^{-1}$) |
|---|---|---|---|---|---|---|
| nHeI[a] | N/A | … | … | … | N/A | 21.3 ± 3.1 |
| As-imp[b] | N/A | … | … | … | … | 9.2 ± 1.1 |
| T500 | 500 | $3.26 \times 10^{19}$[c] | $2.18 \times 10^{-4}$[d] | 0.03 | 4.3 ± 1.4 | 13.9 ± 1.9 |
| T600 | 600 | $5.76 \times 10^{19}$[c] | $8.46 \times 10^{-5}$[d] | 0.09 | 6.3 ± 1.8 | 15.6 ± 2.5 |
| T700 | 700 | $9.10 \times 10^{19}$[c] | $4.59 \times 10^{-5}$[d] | 0.16 | 8.1 ± 2.9 | 18.3 ± 2.6 |
| T800 | 800 | $1.01 \times 10^{20}$[c] | $3.78 \times 10^{-5}$[d] | 0.19 | 14.8 ± 4.8 | 21.0 ± 3.0 |
| T900 | 900 | $8.13 \times 10^{19}$[c] | $2.81 \times 10^{-5}$[d] | 0.26 | … | 22.7 ± 3.3 |
| T1000 | 1000 | $9.04 \times 10^{19}$[c] | $2.38 \times 10^{-5}$[d] | 0.31 | 29.2 ± 5.9 | 20.8 ± 3.7 |

[a]Non-Helium-implanted.
[b]He-implanted with no subsequent annealing processes.
[c]Identically doped films annealed at 30 min per step, Ref. 12.
[d]Reference 12.

constant phonon-boundary scattering mean free path $\Lambda_{p\text{-}b}$, and constant phonon-phonon scattering mean free path $\Lambda_{p\text{-}p}$, resulting in an increased thermal conductivity. Physically, this effect can be explained by the scaling with the diameter of the scattering cross section ($\sim D^2$) and number density ($\sim D^{-3}$) when the total void volume is constant. This leads to stronger phonon scattering from any single void, but a space in which voids are increasingly sparse, the net result being a longer phonon mean free path.

To better simulate 3D geometric scattering effects in a polycrystal, a Monte Carlo ray tracing model was developed to numerically study the dependence of thermal conductivity on a changing distribution of volumetric scattering sites by stochastically calculating the geometric scattering contribution from phonon-grain boundary and phonon-void interactions. The model uses a cross-plane transmission probability calculation after Hori *et al.*[28] and is validated in and between the limits of the thin film and long nanowire, as well as for a cubic polycrystal with varying grain boundary transmission coefficients. Transport through a polycrystalline structure 450 nm in thickness is modelled as three layers of 150 nm-thick grains with lateral dimensions of $50 \times 50$ nm or $80 \times 80$ nm, using a gray approximation transmission coefficient at the grain boundaries and perfectly absorbing film contacts. The grain boundary transmission coefficient is estimated using the form of an empirical model with $\gamma = 2.4$ representing a low-resistance sintered silicon interface,[28] assuming a maximum phonon frequency of $\omega_{max} \sim 15$ THz and a representative phonon frequency of $\omega_{gray} \sim 2.5$ THz corresponding approximately to 50% accumulation of bulk thermal conductivity in room-temperature silicon (estimated from Refs. 29 and 30)

$$t_{gray} = \frac{1}{\gamma \omega_{gray}/\omega_{max} + 1}. \tag{3}$$

Voids are re-oriented randomly each time a simulated phonon passes into a new grain to reduce position bias and more accurately simulate a random distribution of voids at the polycrystal level. Simulations were repeated three times to calculate mean and standard deviation (which was within the height of the markers). Thermal conductivity is calculated using model data for comparably doped bulk silicon[31] ($\sim 38.6$ W m$^{-1}$ K$^{-1}$ at $4.4 \times 10^{20}$ cm$^{-3}$ boron concentration) to determine an intrinsic room temperature phonon-phonon scattering mean free path. The phonon dispersion model properties ($C_v = 0.93 \times 10^6$ J m$^{-3}$ K$^{-1}$ and $v = 1804$ m s$^{-1}$) from Chen[32] are used to neglect contributions to heat transfer from optical phonons resulting in an intrinsic mean free path estimate of $\Lambda_{p\text{-}p} = 69$ nm, which is combined with the total phonon-grain boundary and phonon-void scattering contribution from Monte Carlo using Matthiessen's rule to calculate thermal conductivity

$$k = \frac{1}{3} C_v v \left( \frac{1}{\Lambda_{p\text{-}p}} + \frac{1}{\Lambda_{GB+voids}} \right)^{-1}. \tag{4}$$

Experimental and numerical thermal conductivity data for films undergoing the thermal annealing sequence are plotted in Fig. 3(a). A rise in thermal conductivity as the void distribution trends toward fewer, larger voids in the grain volume is observed in both the numerical and experimental data although with clearly different slopes. Additional mechanisms thought to contribute to the thermal transport, and steeper slope observed in the experimental data include defect evolution at the grain boundaries and precipitation of volumetric boron impurities, though direct data to quantify these contributions were not available. The impact of void morphology on simulated conductivity data, while still present, is less significant under the assumption of smaller lateral grain dimensions (50 nm vs. 80 nm), as grain boundary scattering increases. In Fig. 3(b), we compare the results of the present study with reported silicon-based nano-featured thermoelectric materials[5,33–36] in the thermal conductivity vs. power factor space. It is not appropriate to extract a true material $zT$ from the films of this study considering in-plane power factor and cross-plane thermal conductivity measurements. However, we can estimate a lower bound for in-plane $zT$ as the smaller lateral grain size can be reasonably expected to further reduce in-plane thermal transport. Iso-$zT$ lines for 0.05, 0.10, 0.25, and 1.0 at 300 K are plotted for reference. The films we report occupy a gap region of thermal conductivity between typical thin-film silicon materials[33,35,36] and high-performance nanowires[5,34] due to a combination of high doping, defects/voids, and modest grain size. Samples T900 and T1000, in particular, show strong performance compared to

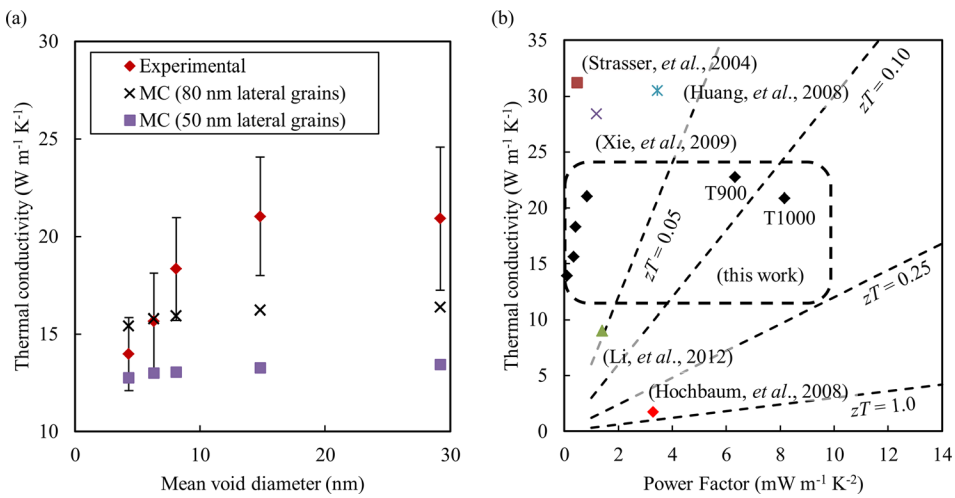


FIG. 3. Comparison of (a) measured thermal conductivity to Matthiessen's rule/Monte Carlo (MC) models for 50 and 80 nm lateral grain size and (b) present study experimental results and nano-featured silicon thermoelectric materials from the literature.

thin film silicon in the thermoelectric literature. Despite no longer benefiting significantly from phonon-void scattering contributions, the jump in thermoelectric power factor and lower thermal conductivity due to high doping levels and small grain structure enhance their position in the $zT$ space.

In conclusion, we report experimental measurements showing reduced thermal conductivity in highly doped polysilicon thin films with high power factors favorable for thermoelectric applications. The films were processed by helium ion implantation and subsequent thermal annealing to produce an evolving distribution of nanoscale voids in the grains. Wide- and small-angle X-ray scattering (WAXS/SAXS) measurements were performed to quantify the void size distributions in the films, which were then used with Matthiessen's rule and Monte Carlo simulations to verify the trends observed in thermal conductivity measurements from time-domain thermoreflectance (TDTR). We find that the thermal conductivity is initially reduced after ion implantation and positively correlated with increasing mean void diameter but is restored to non-He-implanted levels at the point that power factor rises significantly. We suggest that it may be possible to align the observed thermal conductivity suppression and power factor rise by altering the ion implantation sequence for a significant rise in material $zT$.

M.T.D. acknowledges the partial support of this work by the United States Department of Defense through the National Defense Science and Engineering Graduate Fellowship program, and partial support received from the National Science Foundation, grant CBET-1336734. B.L. and D.N. acknowledge the partial support received by FP7-NMP-2013-SMALL-7 in the frame of SiNERGY (Silicon Friendly Materials and Device Solutions for Microenergy Applications) Project, Contract No. 604169.

[1]M. Zebarjadi, K. Esfarjani, M. S. Dresselhaus, Z. F. Ren, and G. Chen, Energy Environ. Sci. **5**, 5147 (2012).
[2]D. Dávila, A. Tarancón, C. Calaza, M. Salleras, M. Fernández-Regúlez, A. San Paulo, and L. Fonseca, Nano Energy **1**, 812 (2012).
[3]X.-Q. Wang and A. S. Mujumdar, Int. J. Therm. Sci. **46**, 1 (2007).
[4]A. I. Boukai, Y. Bunimovich, J. Tahir-Kheli, J.-K. Yu, W. A. Goddard, and J. R. Heath, Nature **451**, 168 (2008).
[5]A. I. Hochbaum, R. Chen, R. D. Delgado, W. Liang, E. C. Garnett, M. Najarian, A. Majumdar, and P. Yang, Nature **451**, 163 (2008).
[6]Y. Li, K. Buddharaju, N. Singh, and S. J. Lee, J. Electron. Mater. **42**, 1476 (2013).
[7]J. Fang and L. Pilon, J. Appl. Phys. **110**, 064305 (2011).
[8]D. Song and G. Chen, Appl. Phys. Lett. **84**, 687 (2004).
[9]J.-K. Yu, S. Mitrovic, D. Tham, J. Varghese, and J. R. Heath, Nat. Nanotechnol. **5**, 718 (2010).
[10]W. Fukarek and J. Kaschny, J. Appl. Phys. **86**, 4160 (1999).
[11]E. Oliviero, S. Peripolli, L. Amaral, P. F. P. Fichtner, M. F. Beaufort, J. F. Barbot, and S. E. Donnelly, J. Appl. Phys. **100**, 043505 (2006).
[12]B. Lorenzi, D. Narducci, R. Tonini, S. Frabboni, G. C. Gazzadi, G. Ottaviani, N. Neophytou, and X. Zianni, J. Electron. Mater. **43**, 3812 (2014).
[13]B. Lorenzi, S. Frabboni, G. C. Gazzadi, R. Tonini, G. Ottaviani, and D. Narducci, J. Electron. Mater. **43**, 3852 (2014).
[14]N. Neophytou, X. Zianni, H. Kosina, S. Frabboni, B. Lorenzi, and D. Narducci, Nanotechnology **24**, 205402 (2013).
[15]D. Narducci, B. Lorenzi, X. Zianni, N. Neophytou, S. Frabboni, G. C. Gazzadi, A. Roncaglia, and F. Suriano, Phys. Status Solidi A **211**, 1255 (2014).
[16]D. Narducci, E. Selezneva, G. Cerofolini, S. Frabboni, and G. Ottaviani, J. Solid State Chem. **193**, 19 (2012).
[17]A. Sood, J. Cho, K. D. Hobart, T. I. Feygelson, B. B. Pate, M. Asheghi, D. G. Cahill, and K. E. Goodson, J. Appl. Phys. **119**, 175103 (2016).
[18]J. Cho, D. Francis, P. C. Chao, M. Asheghi, and K. E. Goodson, J. Heat Transfer **137**, 071303 (2015).
[19]M. N. Luckyanova, J. Garg, K. Esfarjani, A. Jandl, M. T. Bulsara, A. J. Schmidt, A. J. Minnich, S. Chen, M. S. Dresselhaus, Z. Ren, E. A. Fitzgerald, and G. Chen, Science **2360**, 936–939 (2012).
[20]J. Cho, Y. Li, W. E. Hoke, D. H. Altman, M. Asheghi, and K. E. Goodson, Phys. Rev. B - Condens. Matter Mater. Phys. **89**, 115301 (2014).
[21]D. G. Cahill, Rev. Sci. Instrum. **75**, 5119 (2004).
[22]W. S. Capinski and H. J. Maris, Rev. Sci. Instrum. **67**, 2720 (1996).
[23]O. W. Käding, H. Skurk, and K. E. Goodson, Appl. Phys. Lett. **65**, 1629 (1994).
[24]K. E. Goodson, M. I. Flik, L. T. Su, and D. A. Antoniadis, IEEE Electron Device Lett. **14**, 490 (1993).
[25]H.-J. Kim and C. V. Thompson, J. Electrochem. Soc. **135**, 2312 (1988).
[26]B. Zhou, F. Liu, J. Gu, Q. Zhang, Y. Zhou, and M. Zhu, Thin Solid Films **501**, 113 (2006).
[27]R. E. I. Schropp, M. K. van Veen, C. H. M. van der Werf, D. L. Williamson, and A. H. Mahan, MRS Proceedings **808**, A8–4 (2004).
[28]T. Hori, J. Shiomi, and C. Dames, Appl. Phys. Lett. **106**, 171901 (2015).
[29]K. T. Regner, D. P. Sellan, Z. Su, C. H. Amon, A. J. H. McGaughey, and J. Malen, Nat. Commun. **4**, 1640 (2013).
[30]B. Liao, B. Qiu, J. Zhou, S. Huberman, K. Esfarjani, and G. Chen, Phys. Rev. Lett. **114**, 115901 (2015).
[31]W. Liu, K. Etessam-Yazdani, R. Hussin, K. E. Goodson, and M. Asheghi, IEEE Trans. Electron. Devices **53**(8), 1868 (2006).
[32]G. Chen, Phys. Rev. B **57**, 14958 (1998).
[33]M. Strasser, R. Aigner, C. Lauterbach, T. F. Sturm, M. Franosch, and G. Wachutka, Sens. Actuators, A **114**, 362 (2004).
[34]Y. Li, K. Buddharaju, B. C. Tinh, N. Singh, and S. J. Lee, IEEE Electron Device Lett. **33**, 715 (2012).
[35]I. Y. Huang, J. C. Lin, K. D. She, M. C. Li, J. H. Chen, and J. S. Kuo, Sens. Actuators, A **148**, 176 (2008).
[36]J. Xie, C. Lee, M.-F. Wang, Y. Liu, and H. Feng, J. Micromech. Microeng. **19**, 125029 (2009).