Dielectric barrier layers by low-temperature plasma-enhanced atomic layer deposition of silicon dioxide

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ABSTRACT

Electrothermal measurement techniques often require thin dielectric barriers to isolate active electrical test structures from samples of interest. The combined need for electrical passivation but thermal proximity necessitates the use of an electrically thick but thermally thin barrier layer. Here, we demonstrate a hybrid approach toward constructing sub-300 nm SiO\textsubscript{2} multilayer barriers based upon low-temperature plasma-enhanced atomic layer deposition and high density plasma chemical vapor deposition. Using pairs of buried metal test structures, we quantify changes in device resistance and cross-talk after covering the dielectric barrier with thin evaporated gold films and thick electroplated copper films. We show that a hybrid approach to passivating electrothermal measurement devices outperforms individual homogenous barriers formed by either deposition technique.

1. Introduction

Electrothermal measurement devices use metal thermal transducers (i.e. heaters) and metal thermal sensors (i.e. thermometers) to measure the thermal properties of bulk materials, thin films, and nanostructures [1–6]. Metal heaters generate Joule heating when driven with an electrical current, and metal thermometers use changes in electrical resistance to measure the associated temperature fields. These devices require well-controlled, isolated electrical pathways to accurately correlate the measured electrical signals to the thermal signals of interest. For dielectric samples and substrates, the heaters and thermometers can be in intimate contact with the sample material without electrical interference. However, when the samples are electrically conductive, such as semiconductors, metals, ionic solutions, and conductive polymers, the patterned test structures must be electrically-isolated from the sample. Thin film barrier layers are chosen for this role and are widely used to protect electronic devices from a variety of harsh operating conditions that include corrosive working fluids, oxidizing and reducing environments, and high electric fields.

Silicon is readily passivated through self-oxidation, but many other materials require the deposition of dielectric thin film barriers, ranging from high-κ dielectrics (e.g. HfO\textsubscript{2} [7, 8]) to two-dimensional layered films (e.g. hexagonal boron nitride [9, 10]). Atomic layer deposition (ALD) is commonly used to deposit dense thin films for applications ranging from corrosion resistance of metals to dielectric barriers in microelectronic devices [11]. Furthermore, ALD can produce conformal films when depositing onto high aspect ratio device features [12]. For electrothermal devices, the barrier layer must satisfy two criteria: (1) be electrically thick to prevent both DC (resistive) and AC (capacitive, inductive) coupling contributing to signal loss, and (2) be thermally thin to preserve thermal measurement sensitivity to the material properties of interest. The first criterion is achieved by using a fully-densified, homogeneous, and pin-hole free dielectric film. The second criterion is achieved by minimizing the thermal resistance of this dielectric film by reducing the film thickness and/or by choosing a dielectric with sufficiently high thermal conductivity. In amorphous dielectrics frequently chosen for barrier applications, thermal conductivity scales with atomic density [13, 14]. For example, varying the deposition temperature of ALD processes has been shown to induce changes in Al\textsubscript{2}O\textsubscript{3} film density by 15%, with a corresponding change in thermal conductivity of nearly 35% [15]. Such changes in SiO\textsubscript{2} films could reduce the thermal conductivity from 1.4 W/(m-K) at full density to 0.9 W/(m-K) and may impact the sensitivity of some electrothermal measurements. Therefore, both criteria benefit from increasing atomic density of barrier layers, a property often limited by the deposition method and process temperature (see Fig. 1) as well as post-deposition.

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In this article, we characterize the electrical isolation performance of high-quality silicon dioxide ($\text{SiO}_2$) multilayered barriers deposited using both low-temperature plasma-enhanced atomic layer deposition and high density plasma chemical vapor deposition processes. Silicon dioxide is an attractive barrier material due to its chemical inertness, optical transparency, and conventional integration with microfabrication. We assess the passivation characteristics using electrothermal test structures originally designed to measure thermophysical properties of nanostructured metal thin films [16, 17]. In brief, the test structures are fabricated onto a fused silica wafer using optical lithography, electron beam evaporation, and liftoff to pattern 5/60 nm of Ti/Pt into lines (1000 μm long, 5 μm wide) and are configured for four-point resistance measurements. The wafer is diced into chips that each contain two test structures. The devices are then passivated using treatments such as annealing.

![Fig. 1. (a) Wet etch rate of SiO$_2$ films in 200:1 HF grown by HDPCVD, PEALD, PECVD, and thermal oxidation in order of increasing deposition temperature. (b, c) Scanning electron microscopy images of a patterned metal line covered by a single layer of SiO$_2$ deposited by PEALD at an elevated temperature of 270 °C (b) as-fabricated and (c) after driving the device with a sinusoidal current to induce temperature oscillations.](image-url)

In contrast, PEALD of SiO$_2$ does not contain an etch component and relies upon self-limiting surface reactions that are ideally suited to provide conformal and pin-hole free coverage of high aspect ratio structures. In this work, the synergistic advantages of multimodal deposition are derived from the complementary capabilities of each technique, and we demonstrate that the multilayered barriers outperform the equivalent homogeneous layers of either PEALD or HDPCVD SiO$_2$.

2. Experimental details

All PEALD SiO$_2$ films are deposited at 200 °C in an Ultratech/Cambridge Nanotech Fiji hot-walled reactor using tris(dimethylamino)silyl silane and a remote O$_2$ plasma. Depositions are performed using a continuous 130 sccm Ar carrier flow to promote precursor delivery and purging of reaction byproducts. The oxygen plasma is formed using 50 sccm O$_2$ and 300 W of inductively coupled plasma power. All HDPCVD SiO$_2$ films are deposited at 100 °C using a PlasmaTherm VersaLine tool with an inductively coupled plasma (ICP) using silane and O$_2$ plasma [20]. An additional post-fabrication annealing at 600 °C for 6 mins in a 4% forming gas environment is used in some protocols to further densify the barrier layers and eliminate dangling bonds. All substrates were cleaned in an O$_2$ plasma immediately prior to barrier deposition by either method to remove surface organics and promote barrier adhesion.

Seven SiO$_2$ passivation configurations are examined in the present work, where each configuration is tested on eight test structures (four chips each containing two test structures). Set A contains only a single 215 nm-thick HDPCVD layer. Sets B through G begin with a 30 nm-thick PEALD layer to conformally coat the patterned metal features. A 215 nm-thick HDPCVD layer is added to Sets D through G to thicken the barrier. Sets F and G receive a final 30 nm-thick PEALD layer with the intention of covering any pinholes or other defects in the underlying structure.
HDPCVD layer. Sets C, E, and G undergo additional post-fabrication annealing. A summary of the passivation configurations is given in Fig. 2. Sidewalls of patterned metal lines are assumed to be conformally coated by the PEALD process owing to the small step-height (65 nm) and correspondingly small aspect ratio of the metal line features (< 1:1). Plasma-enhanced atomic layer deposition of SiO2 with comparable process parameters has been shown to conformally coat trench features with aspect ratios > 1:10 and up to 1:60 with process optimization [21, 22]. Similarly, the HDPCVD films used in this study are a factor of ~3.3 times thicker than the metal lines which are assumed to be fully buried. Spectroscopic ellipsometry confirms that the wafer-scale uniformity for each deposition technique is within 2% as shown in Fig. 3. Process uniformity is assessed in a companion study using blanket deposition of SiO2 onto four-inch Si wafers that underwent a wet etch process to remove native oxide immediately prior to deposition. Measurements of thickness by ellipsometry are used to calculate deposition rate.

We test the electrical isolation by depositing metal onto the surface of the barrier layers and measuring changes in the electrical characteristics of the underlying test structures. The metal samples tested here include thin evaporated gold films (~10^5 nm thick). We employ two metrics to quantify the electrical isolation provided by each film as shown in Fig. 4. The first metric is a measurement of DC resistance and AC impedance (at frequency f = 200 Hz) for each device, beginning with a baseline measurement prior to sample deposition and again after each metal sample deposition. In this manner, a differential measurement is made and the resistance is considered stable if there is less than a 2% change relative to the baseline at each stage (“leakage resistance” in Fig. 4c). The second metric is a measurement of the DC resistance between two decoupled test structures on the same chip with a lateral separation of 1000 μm (“coupling resistance” in Fig. 4c). The two test structures are considered to be electrically isolated if < 1 μA of current can pass between the lines for voltages applied up to 10 V. In practice, test structures were observed to either fail or pass in a binary manner; those that failed exhibited coupling resistances of ~0.1–1 kΩ whereas those that passed exhibited coupling resistances > 10 MΩ. Both of these measurements use a four-point configuration driven by a current source (Keithley 6221) with a programmable compliance (set to 10 V), and the voltage is measured using a multimeter (HP 34401A).

3. Results and discussion

The deposition rates of PEALD and HDPCVD differ greatly and highlight their complementary capabilities. Whereas the PEALD process achieves a deposition rate of 1.16 Å/min (for a 30 s cycle time), the HDPCVD deposition rate of 1800 Å/min is more than three orders of magnitude faster. Therefore, while PEALD layers provide conformal coverage with thinner but higher-density SiO2, HDPCVD layers are ideally suited to provide comparatively thick layers of lower-quality SiO2. In this study, poor quality refers to SiO2 layers that are less conformal, have a lower atomic density, and/or contain a greater density of structural and chemical inhomogeneities including pinholes, cracks, hydrogen content, dangling bonds, and other defects. The wet etch rate for each type of SiO2 thin film provides a quantitative metric to compare quality and captures the collective influence of these structural and chemical defects. Etch rates are calculated from thickness measurements using spectroscopic ellipsometry (Woollam M2000) before and after etching in a dilute 200:1 hydrofluoric acid (HF) solution. Fig. 1 presents the wet etch rate of SiO2 as deposited by HDPCVD (100 °C) and PEALD (200 °C) along with layers grown by conventional high temperature PECVD (350 °C) and thermal oxidation (1100 °C) processes. Lower temperature HDPCVD processes produce lower density films with poorer Si–O bonding and higher impurity levels. These properties collectively contribute to increased wet etch rates and poorer dielectric performance. Furthermore, PECVD SiO2 films deposited under low temperature conditions often contain higher concentrations of hydrogen in the form of residual OH that are correlated with increased etch rates in buffered oxide etch (BOE) [23, 24]. It is noteworthy that PEALD enables favorable tradeoffs between wet etch rate and deposition temperature not readily achievable with conventional CVD processes. For example, PEALD SiO2 as-deposited at 200 °C...
achieves a wet etch rate comparable to PECVD SiO2 (14% greater), while reducing process temperature by 150 °C. Furthermore, the PEALD process at 200 °C is CMOS compatible whereas conventional CVD processes with long deposition times or temperatures > 350 °C are generally not CMOS compatible.

Low-temperature processing is also desirable to reduce thermal stresses arising from mismatch in the coefficient of thermal expansion (CTE) between the barrier layer and metal comprising the underlying test structure. In the case of SiO2 over Pt, an estimate of the thermal stresses contributing to barrier cracking (see Fig. 1) and enable stress tuning through process optimization [26].

Fig. 4, sample region). This causes all of the devices from Sets A, B, and C to fail both metrics, indicating that a single SiO2 layer provides incomplete electrical isolation and fails to separate the device layer from the evaporated metal. The metal sample layer reduces the device resistance to only a few Ohms and creates a short-circuit pathway between adjacent devices for all devices in these sets. One device from each of Sets D and E was short-circuited, and one additional chip in Set E had adjacent devices that had become coupled. Only one chip from Set F contained coupled devices, despite no change in resistance of the individual devices, and all devices in Set G survived. A second identical evaporation was then performed on all devices to validate the consistency of the failure mechanism. Only one additional chip (Set F) contained coupled devices after this step, whereas all of the surviving devices remained passivated.

Two chips were then selected from each of Sets D through G (for a total of four individual devices per set), and a ~5 μm copper film was electroplated onto the gold sample film. Potentiostatic electrodeposition of copper was carried out at V = −400 mV (vs. Ag/AgCl) from an aqueous acidic electrolyte (0.6 M CuSO4 + 0.03 M H2SO4, pH = 1.7). The thick copper film has a low resistance and any signal leakage from the device would produce a short-circuit. Only one chip (Set E) failed after this step, whereas the other seven chips retained their device resistance and electrical decoupling (see Fig. 5c). A summary of device performance is shown in Fig. 6. The AC resistances at 200 Hz are found after this step, whereas the other seven chips retained their device resistance to only a few Ohms and creates a short-circuit pathway between adjacent devices for all devices in these sets. One device from each of Sets D and E was short-circuited, and one additional chip in Set E had adjacent devices that had become coupled. Only one chip from Set F contained coupled devices, despite no change in resistance of the individual devices, and all devices in Set G survived. A second identical evaporation was then performed on all devices to validate the consistency of the failure mechanism. Only one additional chip (Set F) contained coupled devices after this step, whereas all of the surviving devices remained passivated.

The baseline resistance is measured for each device and shown in Fig. 5. Three devices were discontinuous due to damage during liftoff. The annealed sets of devices all have a higher baseline resistance than the non-annealed devices. This is likely attributed to the inter-diffusion between the titanium and the platinum at elevated temperature. The first metal sample (5/50 nm Ti/Au) is deposited by electron-beam evaporation through a shadow mask over the center of the chip (see Set A). After evaporation of 5/50 nm Ti/Au. (b) Resistance comparison after electrodeposition of a Cu film onto the Au surface for four devices from each of Sets D through G.
process challenges commonly encountered in achieving barrier protection of electrothermal test structures.

Some of the test structures using bilayer SiO2 films (Sets D and E) fail while others contain complete electrical isolation even with the low-resistance copper samples. The devices using trilayer SiO2 films (Sets F and G) retain their baseline resistance on all devices and remain decoupled on all but one of the chips. Efforts to anneal the SiO2 films are shown to impact the underlying metal structures and increase the device resistance. At non-cryogenic temperatures, there is a positive linear relationship between resistance and temperature in most metals, and this enables metal lines to be used as linear temperature sensors with sensitivity $dR/dT$. Using the definition of the temperature coefficient of resistance, the temperature sensitivity is proportional to the device resistance $R_0$ (at a reference temperature $T_0$) such that $dR/dT = -R_0$. This suggests that the increase in device resistance $R_0$ with annealing may inadvertently increase device sensitivity in electrothermal applications.

Low-temperature processing that is matched across deposition techniques enables the growth of thin multilayer SiO2 barrier layers having minimal residual stresses and without damaging temperature-sensitive devices. The conformal nature of PEALD deposition allows for thin film growth onto high aspect ratio features but is generally limited in total thickness. The HDPCVD deposited films are of comparatively lower quality but allow for rapid thickening of the underlying PEALD layers. An idealized homogenous barrier layer increases the effective defect diffusion length with increasing thickness over which defects must propagate to reach the underlying interface. However, in practice, barrier layer failure often initiates at non-homogenous regions including defects and interfaces that are present in any real sample. Upon reaching the underlying metal-barrier interface, defects generally propagate more rapidly leading to accelerated failure. When used individually, thin and high-density PEALD barrier layers offer increased thermal conductance and coverage of high-aspect ratio topology but present a minimal bulk diffusion length. When used in a multilayer, they can additionally close pinhole defects, blunt the propagation of structural defects between adjacent layers, and slow bulk diffusion by imposing the need for lateral diffusion among multilayer interfaces before continued cross-plane diffusion can resume. In contrast, thicker and lower-density barrier layers offer decreased thermal conductance but can increase the effective bulk diffusion length.

4. Conclusion

This work demonstrates the rational design of multilayer barrier layers using the synergistic advantages of different thin film deposition techniques. The combination of PEALD and HDPCVD offers performance increases and enables low temperature (< 200 °C) hybrid multilayer barriers of SiO2. These films are critical to the function of electrothermal measurement platforms and other devices that have strict electrical isolation requirements. All of the SiO2 films deposited using either PEALD or HDPCVD fail to isolate the devices from evaporated metal films, whereas the hybrid approach offers nearly complete passivation even with thick copper films on the surface. This strategy of hybrid films can be extended to other combinations of thin films and/or deposition techniques to achieve functionality and performance exceeding that of the constituent layers alone.

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References


