Effect of Microscale Thermal Conduction on the Packing Limit of Silicon-on-Insulator Electronic Devices

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Abstract—**Silicon-on-insulator (SOI) electronic circuits have a buried silicon dioxide layer which inhibits device cooling and reduces the thermal packing limit, the largest number of devices per unit substrate area for which the device operating temperature is acceptably low. Thermal analysis yields the packing limit of SOI MOSFET devices in terms of the targeted channel-to-substrate thermal conductance. Thermal conduction is microscale if it is significantly reduced by the boundary scattering of heat carriers, phonons in silicon and electrons in aluminum. Microscale effects are negligible above room temperature, but may reduce the packing limit by 44 % for a substrate temperature of 77 K.**

NOMENCLATURE

A	Length satisfying $A >> w$ and $A >> d_{lo}$, (4), m.
A_f	Fin cross-sectional area, m^2.
C	Specific heat per unit volume, J m^{-3} K^{-1}.
D	Packing limit, devices cm^{-2}.
d	Layer thickness, m.
d_e	Thickness of additional silicon dioxide layer, m.
d_{lo}	Local thickness of silicon dioxide between fin and substrate, m.
$G = P/(T_c - T_0)$	Channel-to-substrate thermal conductance, W K^{-1}
h	Heat transfer coefficient, W m^{-2} K^{-1}.
I	Current, A.
k	Thermal conductivity, W m^{-1} K^{-1}
k_{eff}	Effective thermal conductivity, W m^{-1} K^{-1}.
L_d	Separation between gate and metal interconnect, m.
L_g	Half-length of gate in X direction, m.
L_m	Half-length of interconnect between devices in Y direction, m.
$m = (hp/kA)^{1/2}$	Inverse thermal healing length, m^{-1}.
P	Device power, W.
p	Fin perimeter exposed to heat transfer coefficient h, m.
q''	Heat flux, W m^{-2}.
S	Parameter, (3).
T	Temperature, K.
T_0	Substrate temperature, K.
T_f	Fin temperature averaged across width w, K.
T_c	Channel temperature, K.
V	Voltage, V.
v	Carrier velocity, m s^{-1}.
W_0	Separation between devices in Y direction.
w	Fin width normal to heat flow in $X-Y$ plane, m.
w_d	Width of device in Y direction, m.
w_m	Width of metal interconnect in Y direction, m.
X	Coordinate in plane of substrate, m.
Y	Coordinate in plane of substrate, m.
y	Coordinate across film width, m.
Z	Coordinate normal to plane of substrate, m.
Z_1, Z_2, Z_3, Z_4	Constants, (15)–(19).
δ	Parameter, (2) and (3).
Λ	Carrier mean free path, m.
ρ	Electrical resistivity, Ω m.

Subscripts

- d Property or parameter of the source and drain.
- g Property or parameter of the gate.
- m Property or parameter of the metal interconnect.
- o Property or parameter of the implanted silicon dioxide layer.

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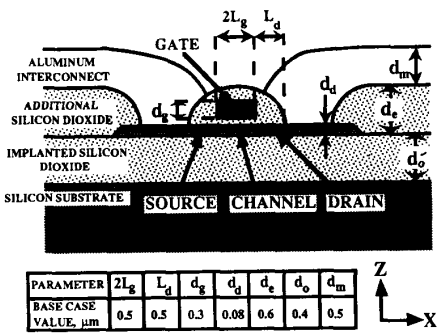
I. INTRODUCTION

CONVENTIONAL electronic devices made of doped silicon are in direct electrical and thermal contact with the silicon substrate. Novel silicon-on-insulator (SOI) electronic circuits have an electrically insulating silicon dioxide layer between the devices and the silicon substrate. Fig. 1 is a schematic of a SOI MOSFET, which is one of the most promising SOI devices [1]. The buried silicon dioxide layer, which is fabricated by implanting oxygen ions in single crystal silicon, electrically isolates neighboring devices, preventing latchup and current leakage. It also improves the operating



PARAMETER	$2L_g$	L_d	d_g	d_d	d_e	d_o	d_m
BASE CASE VALUE, μm	0.5	0.5	0.3	0.08	0.6	0.4	0.5

Fig. 1. Side view of a SOI MOSFET. The source and drain are single crystal, heavily doped silicon. The gate is heavily doped polycrystalline silicon.

speed by reducing the parasitic capacitance of the substrate. However, the implanted silicon dioxide layer possesses a low thermal conductivity, ~ 1 W m^{-1} K^{-1} at room temperature, thus inhibiting conduction cooling of the devices. As a result, thermal conduction to the metal interconnects is an important cooling mechanism whose effectiveness decreases as the length of interconnects between devices, such as neighboring devices in a logic gate, is reduced. Increasing the device packing density, i.e., the number of devices per unit substrate area, can, therefore, reduce the channel-to-substrate thermal conductance, G. The thermal conductance is the ratio of the device power, and the channel-to-substrate temperature difference. The temperature dependence of electromigration in interconnects and hot carrier effects and channel mobilities in devices makes G an important parameter for the design of reliable, high performance SOI circuits. This paper provides an estimate of the relationship between G and the packing density, indicating the largest packing density, or the packing limit, which can result in a targeted value of G.

In the thinnest SOI devices, where the source and drain thicknesses may eventually be as small as $d_d = 0.03$ μm, thermal conduction from the channel may also be reduced by heat carrier-boundary scattering in the source, gate, drain, and metal interconnects. Thermal conduction in a thin bridge is microscale if it is reduced significantly by the scattering of the carriers of heat on its boundaries [2]. Phonons, the quanta of lattice waves, are the dominant carriers of heat in doped silicon, and electrons are the dominant carriers of heat in aluminum. If the thermal conduction is microscale, the effective thermal conductivity along the bridge decreases with decreasing layer thickness. For the first time, this paper investigates the effect of microscale thermal conduction on the thermal packing limit of SOI electronic devices.

The steady-state temperature distribution in a linear array of connected SOI MOSFET devices is calculated by modeling the source, drain, gate, and metal interconnects as cooling fins which conduct the heat dissipated in the channel away from the device. The channel-to-substrate thermal conductance is related to the device separation, and the packing limit is determined as a function of the targeted value of this conductance. The effective thermal conductivity along each fin considering boundary scattering is determined as a function of its bulk thermal conductivity, thickness, and temperature using kinetic theory and the approximate relations of Flik and Tien [3]. The effect of microscale thermal conduction on the packing limit is investigated by comparing microscale predictions which employ the reduced, effective thermal conductivities to *macroscale* predictions which employ the bulk conductivities.

This paper investigates the impact of one of the primary obstacles to the reliable operation of SOI electronic circuits, the high thermal resistance of the implanted silicon dioxide layer. The channel and maximum interconnect temperatures are related to the implanted layer thickness and device parameters, which will facilitate the estimation of the mean time to failure of a circuit from electromigration theory and data. This thermal analysis is required for an optimization of the implanted layer thickness considering the thermal resistance of the layer and its effect on the parasitic capacitance of the substrate. Low-temperature semiconducting electronics possess great potential because of the low electrical resistivity of semiconductors at low temperature and the possibility of hybrid superconductor–semiconductor circuits. This paper demonstrates the importance of microscale considerations for the thermal design of low-temperature SOI circuits.

II. Microscale Thermal Conduction in SOI Electronic Circuits

Boundary scattering reduces thermal conduction in a medium when the mean free path of the carriers of heat is of the order of or larger than the smallest medium dimension. Flik *et al.* [2] determined for metals, dielectrics, and semiconductors the approximate regimes of temperature and microstructure dimension for which thermal conduction is microscale. This section determines the temperature dependent mean free path of heat carriers in each SOI circuit material, and compares it with the dimensions of the circuit components made from that material. Theory for the thin film conduction size effect yields the reduced effective conductivities of these circuit components, which in the following section are used to calculate temperature distributions in the device and interconnects.

The materials for SOI circuits include doped single crystal silicon, doped polycrystalline silicon, or polysilicon, silicon dioxide, and aluminum. Electrons are the dominant carriers of heat in the aluminum interconnects. Phonons are the dominant carriers of heat in doped silicon and silicon dioxide. For each medium, kinetic theory relates the mean free path Λ of the dominant heat carrier to the specific heat due to that carrier per unit volume C, the thermal conductivity k, and the speed of the carrier v, by [4]

$$k = \frac{1}{3} C\, v\, \Lambda. \tag{1}$$

The specific heat C in (1) is only that portion of the total specific heat of the material which is brought about by the energy carrier being analyzed. When applying (1) to aluminum, $C = (135 \text{ J m}^{-3} \text{ K}^{-2})\, T$ is the electron specific heat per unit volume, where T is the temperature, $v = 2.0 \times 10^6$ m s^{-1} is the electron Fermi velocity [4], and $k = k_m$ is the temperature dependent thermal conductivity [5].

While these values are for pure aluminum, some aluminum interconnects possess a finite mass percentage of silicon or copper. These impurities reduce the bulk mean free path of electrons and diminish the importance of electron boundary scattering in the interconnects. They also reduce the bulk thermal conductivity, resulting in a slightly lower channel-to-substrate thermal conductance. The effects of impurities in the interconnects on the channel-to-substrate thermal conductance and on the impact of electron boundary scattering should be investigated.

When applying (1) to the doped-silicon source, drain, and gate, k is the phonon conductivity, v is the phonon velocity, well approximated by the speed of sound in silicon, and C is the phonon specific heat per unit volume. The source and drain of the MOSFET are doped single crystal silicon. The gate is doped polycrystalline silicon. Grain boundaries are effective scatterers of phonons, but will not reduce the thermal conductivity unless the phonon mean free path is of the order of the grain size. Transmission electron microscopy of a 0.2-μm doped polycrystalline silicon film indicates that the grain length in the plane of the film is similar to the film thickness after annealing [6]. Thus the thermal conductivity of the gate differs from that of single crystal doped silicon only when the conduction is also reduced by scattering on the boundaries of the gate. To simplify the present analysis, the scattering of phonons on the gate boundaries is assumed to dominate over the scattering on grain boundaries within the gate. This allows the use of values of the conductivity measured in a single crystal to be employed for the polycrystalline gate. The source, drain, and gate of a MOSFET are each heavily doped. The present analysis assumes that they have the same carrier concentration, allowing the use of the same value of the bulk thermal conductivity for these components. The temperature dependent bulk values of the thermal conductivity for the source and drain, denoted by k_d, and the gate, denoted by k_g, are assumed to be those measured in a single crystal of silicon doped with 2.0×10^{19} phosphorus atoms (cm^{-3} [5]. The phonon thermal conductivity and mean free path decrease with increasing carrier concentration in doped semiconductors. The experimental specific heat, which varies little with doping concentration, is taken from [7], and the speed of sound is $v = 6400$ m s^{-1}.

For the silicon dioxide layers, the thermal conductivity k_o and the specific heat C are assumed to be those of fused silicon dioxide [8], [9], and the speed of sound is $v = 5900$ m s^{-1}. The thermal conductivity of the buried silicon dioxide layer, which is fabricated by oxygen ion implantation, has not been measured and may differ substantially from that of fused silicon dioxide due to a potentially different microstructure. The measurements of Schafft *et al.* [10] indicate that the thermal conductivity of CVD silicon dioxide layers at room temperature may be smaller than the values employed here. A lower conductivity in the silicon dioxide layers would result in a lower channel-to-substrate thermal conductance, and therefore, a higher device operating temperature for a given power. The mean free path of phonons in silicon dioxide calculated using (1) is of the order of 1 nm. However, the strong frequency dependence of phonon free paths in amorphous materials makes possible a conduction size effect in a layer even when the mean free path is much smaller than the layer thickness. Goodson and Flik [11] solved the Peierls–Boltzmann phonon transport equation for the case of steady-state conduction normal to an amorphous silicon dioxide layer. They determined that carrier-boundary scattering reduces the effective layer conductivity by less than 12 % for layers thicker than 3000 Å above room temperature. The impact of microscale conduction phenomena within the silicon dioxide is neglected.

TABLE I
BULK THERMAL CONDUCTIVITY VALUES.

Temperature	$k_d = k_g$ W m^{-1} K^{-1}	k_m W m^{-1} K^{-1}	k_0 W m^{-1} K^{-1}
50 K	256	1230	0.340
77 K	373	449	0.530
300 K	120	237	1.38

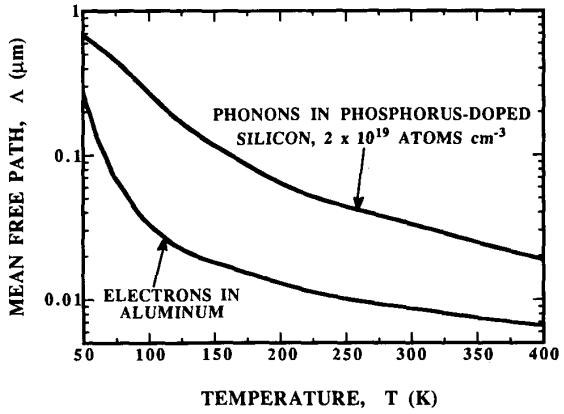


Fig. 2. Mean free paths of electrons in aluminum and phonons in heavily doped silicon.

Values of the bulk thermal conductivity employed at 50, 77, and 300 K are given in Table I. The mean free paths of electrons in aluminum and phonons in doped silicon are shown in Fig. 2. Since a SOI MOSFET may eventually be as thin as 0.02 μm and interconnects can be as thin as 0.5 μm, boundary scattering must be considered, particularly in the source and drain and at low temperatures. Carrier boundary scattering has the greatest impact on thermal conduction in the source and drain of the device.

Flik and Tien [3] developed an approximate theory for the reduction of the thermal conductivity along a film as a function of the ratio of the film thickness d to the carrier mean free path, $\delta = d/\Lambda$. For $d > 1$,

$$\frac{k}{k_\infty} = 1 - \frac{2}{3\pi\delta} \tag{2}$$

where k is the effective conductivity along the thin layer and is the bulk conductivity. For $\delta < 1$

$$\frac{k}{k_\infty} = 1 - \frac{2(1-S^3)}{3\pi\delta} + \frac{2\delta}{\pi}\ln\frac{1+\delta+S}{1+\delta-S} - \frac{2}{\pi}\arccos\delta \tag{3}$$

where $S = (1 - \delta^2)^{1/2}$. The effective thermal conductivities of the doped silicon source, drain, and gate, and the aluminum interconnect are calculated from the bulk values in these materials using (2) and (3) and the mean free paths given in Fig. 2.

Equations (2) and (3) were derived by assuming that carrier scattering on the top and bottom boundaries of the film is diffuse, and by neglecting the transmission of carriers through the boundaries. The use of (2) and (3) also neglects carrier scattering on the side boundaries of a bridge, i.e., on those boundaries parallel to the Z direction in Fig. 1. This is important if the ratio of the carrier mean free path and the microbridge width is of the order of or greater than unity. The doped silicon source and drain and aluminum interconnect widths are 0.8 μm, and the doped polysilicon gate width is 0.5 μm. This condition is satisfied in the interconnects above about 70 K, in the source and drain above about 180 K, and in the gate above about 230 K. Below these temperatures, (2) and (3) overpredict the effective conductivity of the bridge and result in an underestimate of the effect of boundary scattering on the packing limit.

III. Thermal Analysis

The base case dimensions for the present analysis are those of the recently fabricated ultra-thin SOI MOSFET of Woerlee *et al.* [12]. The width of the device normal to Fig. 1 is $w_d = 0.8$ μm. The parameters d_m, d_e, d_g, and L_d are not given in the reference and are estimated as indicated in Fig. 1. The width of the metal interconnects is estimated to be $w_m = w_d = 0.8\mu$m. A typical value of the device operating power calculated from the given current–voltage data is $P = 0.74$ mW for a gate-to-substrate bias of 3 V. For a circuit packaged in a chip, the tops of the devices and interconnects are covered by a thermally insulating layer, typically of silicon dioxide or silicon nitride, which is thicker than the silicon dioxide layer separating the device components and interconnects from the substrate. The tops of the devices are additionally insulated from the chip packaging material by a thick air gap. As a result, almost all of the heat dissipated in the devices travels through the implanted silicon dioxide layer and into the silicon substrate which has a high thermal conductivity.

The present analysis treats the case of steady-state conduction which occurs when neighboring devices are dissipating energy for an extended period. The time required for steady-state to be achieved is of the order of $(d_o)^2/(k/C)$, where k/C is the thermal diffusivity of silicon dioxide, yielding about 200 ns at room temperature. The rate of Joule heating in the source and drain, $2I^2L_d\rho/(wd_d)$, where ρ is the electrical resistivity of the source and drain based on the carrier concentration [13], is nearly two orders of magnitude smaller than the device power and is neglected. Joule heating is also neglected in the aluminum interconnects, which have a larger cross-sectional area and smaller electrical resistivity than the source and drain. The channel is modeled as a heating source of power equal to the device power and is assumed to be isothermal at the temperature T_c. The thickness of the gate oxide was 0.0125 μm [12]. The thermal resistance of this layer is neglected in the present analysis because it is much smaller than the resistance to the flow of heat from within the gate into the substrate.

The substrate temperature is assumed not to vary in the X and Y directions, i.e., the interface between the substrate and the implanted silicon dioxide layer is at a constant temperature, T_0. Define d_{lo} as the local thickness of silicon dioxide separating a component from the substrate. For the interconnects, this parameter is $d_{\text{lo}} = d_o + d_e$, and for the source, channel, and drain it is $d_{\text{lo}} = d_o$. When the gate is not above the channel, it is separated from the substrate by a silicon dioxide layer of thickness approximately equal to $d_{\text{lo}} = d_o + d_e/2$. Thermal conduction in the X direction in the silicon dioxide below the source, drain, and interconnects, and in the Y direction in the silicon dioxide below the gate, is neglected because the ratios $k_o d_{\text{lo}}/(k_m d_m)$, $k_o d_{\text{lo}}/(k_d d_d)$, and $k_o d_{\text{lo}}/(k_g d_g)$ are all much less than unity. The local heat flux from the device or interconnect to the substrate through the silicon dioxide is $h(T - T_0)$, where T is the local device or interconnect temperature. The heat transfer coefficient h is $k_{\text{eff}}/d_{\text{lo}}$, where k_{eff} is an effective thermal conductivity which accounts for conduction in the silicon dioxide.

Conduction in the silicon dioxide is modeled as two dimensional in the plane normal to the direction of heat flow within the component above, e.g., in the $X - Z$ plane for the gate, and in the $Y - Z$ plane for the source, drain, channel, and interconnects. The ratio k_{eff}/k_o is greater than unity and increases with decreasing w/d_{lo}, where w is the width of the fin in the Y direction for the source, drain, channel, and interconnects, and is the width in the X direction of the gate fin. In the limit of $w/d_{\text{lo}} >> 1$, the conduction in the silicon dioxide layer is one dimensional in the Z direction, and k_{eff}/k_o approaches unity. If the fin is assumed to deliver a heat flux q'' to the silicon dioxide which does not vary across the width of the fin, separation of variables yields the average fin excess temperature, $T_f - T_0$ in terms of q'', w, k_o, and $d$lo. Using $k_{\text{eff}} = q'' d_{\text{lo}}/(T_f - T_0)$, the ratio k_{eff}/k_o is

$$\frac{k_{\text{eff}}}{k_o} = \left[\frac{A\, w\, d_{\text{lo}}}{4 \sum_{n=0}^{\infty} \tanh(\lambda_n d_{\text{lo}}) \sin^2(\lambda_n w/2)/(\lambda_n)^3} \right] \qquad (4)$$

$$\lambda_n = \frac{\pi}{2A}(2n+1)$$

where A is a length satisfying $A >> d_{\text{lo}}$ and $A >> w/2$. Equation (4) is approximated by

$$\frac{k_{\text{eff}}}{k_o} = \left[1 - 0.542\,76 \frac{1 - 0.932 \exp\left(-1.538 \frac{w}{d_{\text{lo}}}\right)}{w/d_{\text{lo}}} \right]^{-1} \qquad (5)$$

which is within 0.5 % for $w/d_{\text{lo}} > 0.6$.

Each fin is nearly isothermal across its width w due to the small values of the ratios of the thermal resistances per unit fin length for conduction across the film width and through the underlying silicon dioxide, $(w/kd)/(d_o/k_o w)$, where k is the fin conductivity and d is the fin thickness in the Z direction. This results in a heat flux distribution into the silicon dioxide which is peaked at the side edges of the fin and in a

ratio of k_{eff}/k_o which is larger than that predicted by (4), which assumes the heat flux is uniform over the fin width. The largest error due to the use of (4) is determined using separation of variables and a heat flux distribution proportional to $((w/2)^2 - y^2)^{-1/2}$, where y is the coordinate across the fin width which is zero at the center of the fin. The temperature in the fin increases with the absolute value of y for this heat flux distribution, indicating that k_{eff}/k_o determined in this manner is an upper bound for the correct value. This result differs from (4) by less than 10 % for all values of w/d_{lo}. Since (4) yields a lower bound for k_{eff}/k_o, the error in k_{eff}/k_o due to the use of (4) is less than 10 %.

The thermal boundary resistances of the interfaces of aluminum and silicon with the implanted silicon dioxide layer have not been measured. The measurements of Swartz and Pohl [14] on a variety of metal–dielectric interfaces suggest that boundary resistances at room temperature lie between 10^{-8} m^2 K W^{-1} and 10^{-7} m^2 K W^{-1}, while the smallest value of the silicon dioxide thermal resistance at room temperature is $1/h = d_{\text{lo}}/k_{\text{eff}} = 2.2 \times 10^{-7}$ m^2 K W^{-1}. Due to the lack of experimental data, the present analysis neglects the boundary resistances, although they may significantly reduce the heat transfer coefficient h.

Temperature gradients in the Z direction in the interconnects, source, drain, and gate are neglected. This is justified by the small values compared to unity of the Biot numbers at 300 K for each case, $h_m d_m/k_m = 0.0058$, $h_d d_d/k_d = 0.0034$, and $h_g d_g/k_g = 0.0106$. Temperature gradients in the Y direction in the device and interconnects and temperature gradients in the X direction in the gate are neglected. This simplification allows the source, gate, drain, and interconnects to be treated as one-dimensional fins which enhance the heat transfer from the channel. The fin healing length is defined by $1/m = (hp/kA_f)^{-1/2}$, where k is the thermal conductivity within the fin, A_f is its cross-sectional area, and p is the fin perimeter which is exposed to the heat transfer coefficient h. The ratio of the spatial coordinate in the fin and the healing length is the argument in the exponential functions which solve the fin heat equation. The distance from a heating source over which the fin temperature recovers to the substrate temperature is of the order of the healing length.

A schematic of the thermal model is shown in Fig. 3. The devices are assumed to be in an infinite linear array, each connected by an interconnect of length $2L_m$, and each dissipating the same power P. This idealization results in an estimate of the worst-case temperature distribution in a real circuit for a given value of the minimum device separation, $2L_m$. Two planes of symmetry are illustrated in Fig. 3. These allow the temperature to be calculated between the two planes using adiabatic boundaries at these planes. The temperature and location within the interconnect are given by T_m and the coordinate x_m, the temperature and location within the drain are given by T_d and x_d, and the temperature and location within the gate are given by T_g and x_g.

Although the heat transfer coefficient from the portion of the interconnect over the drain is larger than h_m, the heat transfer from the interconnect is calculated using h_m for all values of x_m. This is justified only if L_m and the thermal healing

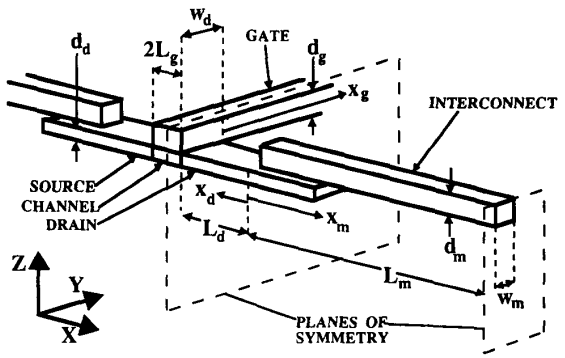


Fig. 3. Schematic of the thermal model.

length in the interconnect, $1/m_m = (k_m d_m/h_m)^{1/2} = 6.6\mu$m at 300 K, are large compared to the length of the overlap. At $x_g \sim 2\mu$m the gate reaches a metal line, which continues for greater x_g separated by $(d_o + d_e)$ from the substrate. In the present approximate analysis, the gate is treated as a doped polysilicon fin of infinite length separated from the substrate by an oxide of constant thickness $(d_o + d_e/2)$, neglecting the variation of h_g and the different properties and dimensions of the metal. The error resulting from this simplification increases with the thermal healing length in the gate, $1/m_g = (k_g d_g/h_g)^{1/2} = 2.9\mu$m at 300 K. The thermal healing length in the drain is $1/m_d = (k_d d_d/h_d)^{1/2} = 1.4\mu$m at 300 K.

The one-dimensional energy equations and boundary conditions are

$$\frac{\partial^2 T_m}{\partial x_m^2} - (m_m)^2(T_m - T_0) = 0 \tag{6}$$

$$\frac{\partial^2 T_d}{\partial x_d^2} - (m_d)^2(T_d - T_0) = 0 \tag{7}$$

$$\frac{\partial^2 T_g}{\partial x_g^2} - (m_g)^2(T_g - T_0) = 0 \tag{8}$$

$$T_m(x_m = 0) = T_d(x_d = 0) \tag{9}$$

$$T_d(x_d = L_d) = T_g(x_g = 0) = T_c \tag{10}$$

$$T_g(x_g \to \infty) = T_0 \tag{11}$$

$$\left(\frac{\partial T_m}{\partial x_m}\right)_{x_m = L_m} = 0 \tag{12}$$

$$-k_m w_m d_m \left(\frac{\partial T_m}{\partial x_m}\right)_{x_m=0} - k_d w_d d_d \left(\frac{\partial T_d}{\partial x_d}\right)_{x_d=0} = 0 \tag{13}$$

$$k_d w_d d_d \left(\frac{\partial T_d}{\partial x_d}\right)_{x_d=L_d} - k_g L_g d_g \left(\frac{\partial T_g}{\partial x_g}\right)_{x_g=0} + h_d w_d L_g (T_c - T_0) = \frac{P}{2}. \tag{14}$$

The solutions to these equations are

$$T_m - T_0 = Z_1 \cosh\left[m_m(L_m - x_m)\right] \tag{15}$$

$$T_d - T_0 = Z_2 \exp\left[m_d x_d\right] + Z_3 \exp\left[-m_d x_d\right] \tag{16}$$

$$T_g - T_0 = Z_4 \exp\left[-m_g x_g\right]. \tag{17}$$

The coefficients Z_1, Z_2, Z_3, and Z_4 are the solutions to (18) (see bottom of the page).

The channel temperature is $T_c = T_g(x_g = 0) = Z_4 + T_0$. The largest temperature in the interconnect is $T_m(x_m = 0) = Z_2 + Z_3 + T_0$, a result of importance to the study of electromigration in SOI interconnects. The channel-to-substrate thermal conductance from one device is defined as

$$G = \frac{P}{(T_c - T_0)} = \frac{P}{Z_4}. \tag{19}$$

IV. Results and Discussion

All of the calculations are performed using the base case dimensions indicated in Fig. 1 and at the beginning of the previous section, unless otherwise indicated. Microscale analysis yields the results in the figures that follow, i.e., the results are calculated using the reduced thermal conductivities given by (2) and (3), unless they are labeled "macroscale," in which case the bulk, unreduced values of the thermal conductivities are used. Although the interconnects and device components have temperatures varying between the substrate temperature T_0 and the channel temperature T_c, the properties employed in the calculations are those for the temperature T_0. Thus the variation of properties with temperature for a given value of T_0 is neglected. The error in the channel-to-substrate conductance due to this approximation increases with $T_c - T_0$, which is proportional to the device power, and is estimated for different substrate temperatures by comparing the conductances calculated using property values at the temperature T_0 with those calculated using property values at the temperature T_c. For $T_c - T_0 = 25$ K, the relative changes in the conductance are 38, 11, and 2.5 % for $T_0 = 50$, 77, and 300 K, respectively. Neglecting the temperature variation of the thermal properties results in the greatest error at low temperatures. The temperature dependence of the mean free path is also neglected, resulting in an overestimate of the impact of microscale conduction phenomena.

For the base case with a substrate temperature of $T_0 = 300$ K and a long interconnect length, $L_m m_m >> 1$, the relative importances of the cooling paths for the heat dissipated in the channel are as follows: 19 % of the heat flows directly from the device through the silicon dioxide layer into the substrate, 25 % flows out through the gate, and 56 % flows out through the metal interconnects. The relative importance of the heat flow through the gate decreases if the device width w is increased.

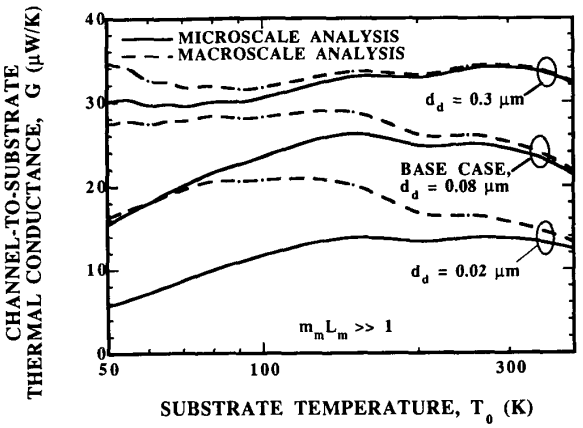


Fig. 4. Microscale and macroscale predictions of the channel-to-substrate thermal conductance.

Microscale and macroscale predictions of the thermal conductance G as a function of temperature and device thickness are shown in Fig. 4. The calculations are for long interconnects, $m_m L_m >> 1$. Macroscale analysis overpredicts the values of the effective thermal conductivity in the fins, and therefore, overpredicts the thermal conductance. The error of the macroscale prediction is small at room temperature, but increases with decreasing temperature due to the increasing mean free paths of both phonons and electrons. The relative error of the macroscale prediction increases with decreasing device thickness.

Fig. 5 shows the effect of finite values of the device separation $2L_m$ on the channel temperature and the maximum interconnect temperature for varying values of the implanted silicon dioxide layer thickness. Both temperatures increase as the device separation is decreased. Both temperatures increase with increasing thickness of the silicon dioxide layer. This figure clearly shows the advantages of thinner silicon dioxide layers for reducing the operating temperature of SOI devices and interconnects.

$$\begin{bmatrix} -m_m k_m d_m w_m \times \sinh(m_m L_m) & m_d k_d d_d w_d & -m_d k_d d_d w_d & 0 \\ 0 & m_d k_d d_d w_d \times \exp(m_d L_d) & -m_d k_d d_d w_d \times \exp(-m_d L_d) & L_g m_g k_g d_g + L_g h_g w_d \\ \cosh(m_m L_m) & -1 & -1 & 0 \\ 0 & -\exp(m_d L_d) & -\exp(-m_d L_d) & 1 \end{bmatrix} \times \begin{bmatrix} Z_1 \\ Z_2 \\ Z_3 \\ Z_4 \end{bmatrix} = \begin{bmatrix} 0 \\ P/2 \\ 0 \\ 0 \end{bmatrix}. \tag{18}$$

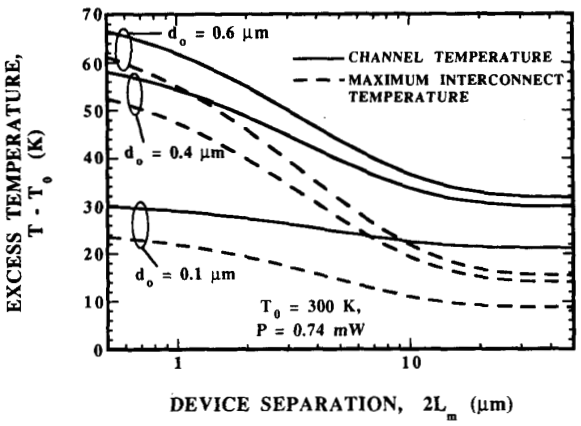


Fig. 5. Dependence of the channel temperature and the maximum interconnect temperature on the interconnect length.

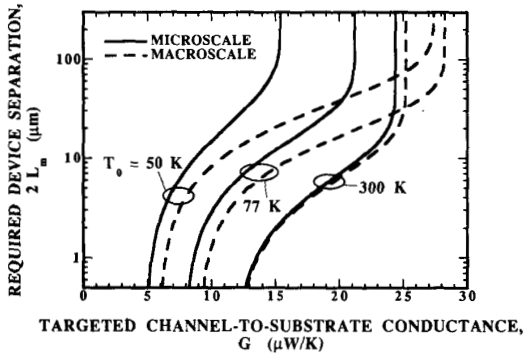


Fig. 6. Microscale and macroscale predictions of the required device separation in terms of the targeted channel-to-substrate thermal conductance.

Fig. 6 shows microscale and macroscale predictions of the required separation between connected devices as a function of the targeted value of G. The large slope of the curves for large values of the device separation shows that beyond a certain separation, of the order of the thermal healing length in the metal, $1/m_m$, additional separation does not enhance the heat transfer from the device. This figure indicates that for a given operating temperature and set of device parameters, there is a limited range of values of G which can be achieved by variation of the device separation alone. It may be impossible to keep the channel temperature below a reliability dictated limit without decreasing the device power. The error in the required device separation due to neglecting microscale effects is small at 300 K but increases with decreasing temperature until it is of great importance at 50 and 77 K. The predictions of microscale and macroscale analyses, which considered the temperature variation of material thermal properties would differ by less than those of the present analysis because the importance of microscale effects in a given component, is reduced as its temperature increases from T_0. The present analysis provides an upper bound for the impact of microscale effects on G.

If the separation between devices in the X direction is $2L_m$ taken from Fig. 6 and in the Y direction is $W_0 = 10\mu$m, the packing limit D can be estimated by using

$$D = \frac{1}{[(2L_m + 2L_d + 2L_g)(w + W_0)]}. \tag{20}$$

TABLE II
MICROSCALE AND MACROSCALE PREDICTIONS OF THE PACKING LIMIT 10^6 DEVICES cm^{-2}

	MICROSCALE	MACROSCALE	MACROSCALE ERROR
$T_0 = 300$ K, $G = 1.85\ \mu$W K^{-1}	1.42	1.52	6.6 %
$T_0 = 77$ K, $G = 11.4\ \mu$W K^{-1}	1.42	2.06	44 %
$T_0 = 50$ K, $G = 7.08\ \mu$W K^{-1}	1.42	2.50	76 %

The error of macroscale predictions of the packing limit are given in Table II. The values of the channel-to-substrate conductance G are chosen such that the packing limit is the same for all three substrate temperatures. Macroscale analysis neglects the reduction of thermal conduction cooling due to heat carrier boundary scattering and overpredicts the packing limit. The error in the macroscale prediction increases with decreasing temperature due to the increasing importance of boundary scattering at low temperatures. The table shows that to achieve the same packing density at cryogenic temperatures in SOI circuits a lower thermal conductance must be targeted.

V. CONCLUSIONS

Microscale thermal conduction in the aluminum interconnects and the doped silicon source, drain, and gate of SOI ultra-thin electronics reduces the packing limit slightly at room temperature and dramatically at low temperatures. For the base case, 81 % of the heat dissipated in the channel flows out through the interconnects and gate of a SOI MOSFET rather than directly down from the device. Reduction of the additional silicon dioxide thickness, d_e in Fig. 1, will enhance this cooling and improve the packing limit.

The optimal oxide layer thickness for SOI electronics should be determined by balancing the competing aims of improved reliability, achieved by decreasing the layer thickness and lowering the operating temperature of the device and metal interconnects, and faster operating speeds, achieved by increasing the layer thickness and reducing the parasitic capacitance of the substrate.

The present steady analysis does not account for the transient operation MOSFET devices. An unsteady analysis of thermal conduction in SOI circuits should be performed, and the influence of temperature fluctuations on the median time to failure of devices and interconnects should be investigated.

Finite element heat conduction analysis packages are expected to become standard elements of computer-aided design tools for the development of integrated circuits. For the design of IC's operating at 77 K, it is recommended to incorporate in these packages the ability to account for size effects on the thermal conductivity. This is imperative for SOI technology,

due to the increased thermal resistance between channel and substrate.

There is a need for the experimental measurement of thin film properties and local temperatures in integrated circuits. Data are required for the thermal resistance normal to the implanted silicon dioxide layer in SOI. In addition, the approximate relations for the size effect on the thin film thermal conductivity, (2) and (3), are supported by very few data. Since they neglect many aspects of microscale conduction, such as the energy dependence of electron and phonon free paths, it is important that more data are gathered on the effective thermal conductivity along thin layers of semiconductors and metals. Data are also required for local temperatures in operating integrated circuits. These data will indicate the accuracy of thermal models such as the one presented here.

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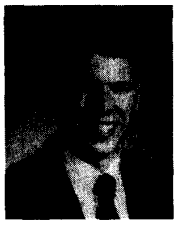

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