

Thermal Mapping of Interconnects Subjected to Brief Electrical Stresses

Y. S. Ju and K. E. Goodson

Abstract—The failure of metal interconnects subjected to brief electrical-current pulses is a reliability concern for the integrated circuits industry, especially in connection with electrostatic discharge (ESD). Since the magnitude and spatial distribution of the temperature rise during pulsing events strongly influence these failures, the development of suitable thermometry techniques is needed to understand the failure. This work reports scanning laser-reflectance thermometry with a novel calibration procedure, which captures transient temperature distributions along interconnects subjected to sub-microsecond current pulses. The temperature distribution is strongly affected by corners and contact pads and by the pulse duration.

I. INTRODUCTION

THE THERMAL characteristics of many microdevices, such as the maximum temperature rise and the spatial temperature distribution, are important figures of merit for the design process. Thermal characterization is of particular importance for metal interconnects in VLSI circuits, because their reliability can be strongly influenced by temperature fields. The median time to failure of metallization due to electromigration decreases rapidly with increasing temperature and current density [1]. Also important are spatial temperature gradients [2], which can affect the median time to failure. Interconnects fail due to brief, high-current pulses encountered during initialization of field-programmable gate arrays [3], [4] and electrostatic discharge (ESD) [5], [6]. While the exact failure mechanism is not well understood, melting and delamination of interconnects and the fracture of the surrounding passivation have been considered responsible.

Interconnect thermometry is required to investigate the failure mechanisms and to identify possible threshold temperatures and current densities for their occurrence. One method for measuring the temperature of VLSI interconnects is to monitor their temperature-dependent electrical resistance (e.g., [5], [6]), which yields the spatially-averaged temperature rise along the interconnects. Several optical methods, including infrared thermography [7], fluorescence thermography [8], and laser-reflectance thermometry [9] offer the advantage of the ability to spatially map the temperature distribution. The temperature rise can vary significantly within an interconnect because of nonuniform heating induced by contacts, corners,

Manuscript received May 30, 1997. The work of K. E. Goodson was supported by the Semiconductor Research Corporation through Contract 97-SJ-461, and the ONR Young Investigator Award. The work of Y. S. Ju was supported by the affiliate companies of the Center for Integrated Systems at Stanford University.

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Publisher Item Identifier S 0741-3106(97)08098-1.

and vias. Although the temperature distribution can also vary dramatically depending on the duration of the electrical stress, the transient thermal mapping of interconnects has received little attention.

This manuscript reports short-timescale spatial mapping of temperature fields in unpassivated interconnects subjected to current pulses of duration as brief as 200 ns. The measurements are performed using a scanning laser-reflectance thermometry technique, which determines local temperature changes in VLSI circuit samples by monitoring the transient surface reflectance.

II. EXPERIMENTS

The experimental apparatus integrates scanning laser optics with an electrical probe station and is described in detail elsewhere [10]. A key parameter in the calibration of this thermometry technique is the thermorelectance coefficient, C_{TR} , which is the relative change of the optical reflectance per unit change in the surface temperature. The thermorelectance coefficient depends on the material being interrogated as well as the wavelength of the probe beam. Typical values for metals and semiconductors in the visible wavelength range are $10^{-5} \sim 10^{-4} \text{ K}^{-1}$. Metallization in modern VLSI circuits consists of alloys, whose optical properties are rarely known with the necessary accuracy. For this reason, a calibration procedure is essential for each metallization sample.

Previous thermorelectance studies used a uniformly-heated large area sample for calibration. However, when an optical lens system with a high numerical aperture and shallow depth of focus is used, which is the case for VLSI circuit elements, systematic errors can result from the thermal expansion of a heater-sample assembly. In order to avoid this problem, we have developed a two-step calibration method employing interconnect structures both as heaters and electrical resistance thermometers [11]. The calibration uses 1500- μm long interconnects, which are very nearly isothermal when subjected to electrical heating pulses. The temperature derivative of the electrical resistance of the interconnects is calibrated using a temperature-controlled wafer holder. The thermorelectance coefficients are obtained by comparing the changes in the surface reflectance with the changes in the electrical resistance while subjecting the interconnects to electrical heating pulses. Electrical pulses of duration between 10 and 100 μs are applied during the calibration. The incident probe laser beam power is less than 1 mW.

The interconnect structures studied here are made of Al-Cu-Ti alloy and are 4 μm wide and 0.5 μm thick. The

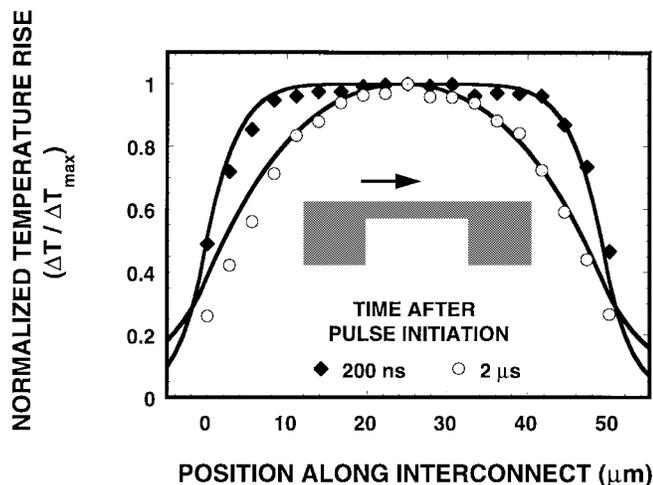


Fig. 1. Comparison of the shapes of the temperature rises along the 50- μm long straight interconnects subjected to electrical pulses of durations 200 ns and 2 μs .

underlying passivation is a polymer layer capped with a 0.25- μm silicon dioxide buffer layer. Repetitive electrical pulses from a pulse generator are applied to the interconnects while a focused laser beam is scanned along the length of the line, x . The rise time of the pulse is 50 ns and the pulse repetition rate is 100 Hz. The low duty cycle eliminates the residual temperature rise between successive pulsing. At each scan point, temperature rise is recorded as a function of the time after pulse initiation t .

III. RESULTS

Fig. 1 compares the shapes of temperature rise distributions along the straight interconnects subjected to electrical heating pulses of durations 200 ns and 2 μs . The temperature distributions become more rounded with increasing time after the pulse initiation. This is because the interconnect ends are anchored near the initial temperature due to their proximity to the contacts, which are not significantly heated. At a given time t , the influence of the lower temperature end conditions propagates inward over a length comparable to the heat diffusion length along the interconnect. The relevant heat diffusion lengths, $L_D = (\alpha t)^{1/2}$, where α is the thermal diffusivity of the aluminum alloy, are 4 and 13 μm for $t = 200$ ns and 2 μs , respectively. For the largest value of t , the data are relatively independent of x only along a small portion of the interior of the line. Also shown are the predicted spatial temperature profiles, which are obtained from a numerical solution to the heat conduction equation. The cross-sectional temperature distribution of the metal at each location along the interconnect is assumed to be uniform and the heat conduction through the underlying passivation layer in the direction along the interconnects is neglected.

The inset in Fig. 2 shows the interconnect structures with sharp corners. Due to current crowding, the heat generation rate per unit volume is highly peaked at the inner portion of the corner, which influences the temperature distribution at short times after the heating pulse initiation. Fig. 2 shows the shape of the temperature distribution along the diagonal of the

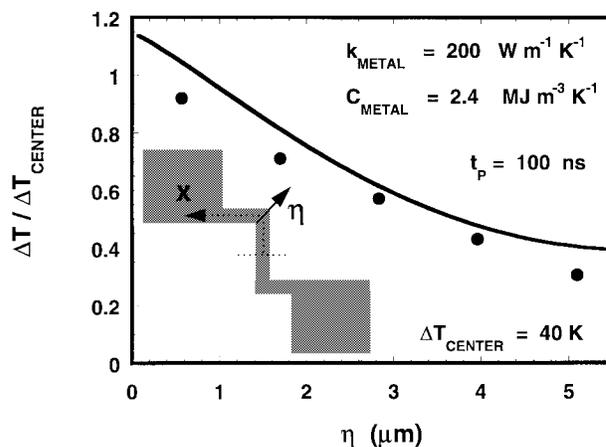


Fig. 2. The shape of the temperature rise along the diagonal of the corner at the time $t = 100$ ns after the pulse initiation. The temperature rise is compared with ΔT_{CENTER} , which is the temperature rise at the center of the interconnect.

corner (η) at the time $t = 100$ ns after the initiation of the pulse. The temperature rise decreases toward the outer part of the corner. The temperature rise is compared with that at the center of the interconnect structures at $x = 0$, ΔT_{CENTER} . The effect of nonuniform heating diminishes as the heat diffusion length becomes much larger than the interconnect width. The corner region becomes nearly isothermal at the end of the heating pulses of duration near or larger than 1 μs . A recent publication showed that the temperature variation at the corner for pulses of duration 250 ns causes extrusion failure to begin at $\eta = 0$ [11].

The temperature distribution at the corner is predicted by first solving the Poisson equation, which yields the current distribution and, hence, the volumetric heat generation rate. In the present study, the two-dimensional heat conduction equation is solved for the metal, whose boundaries are assumed to be adiabatic. The heat diffusion into the passivation layer and the temperature dependence of the electrical resistance are neglected. Fig. 2 shows reasonable agreement between the prediction and the data. The discrepancy can be explained by the larger heat loss to the underlying passivation layer at the outer part of the corner. The change in the current distribution due to the temperature dependent electrical resistance also influences the resulting temperature profiles. The analysis and data in Fig. 2 shows that thermal failure due to current crowding is important for pulses briefer than the heat diffusion time across the diagonal, which is near 200 ns here.

Fig. 3 shows temperature distributions measured along the centerline, that is, along the x coordinate of the interconnects with sharp corners. The shapes of the distributions are strongly influenced by the corners and the time after pulse initiation. The average temperature rise at the corner of the interconnects is smaller than that at the straight portion because of the smaller average power dissipation and a larger contact area with passivation layers. A minimum in the temperature rise exists at the center of the corner shortly after the initiation of pulses. As more time elapses after the initiation of the pulse, heat diffusion into the unheated contact pads becomes more

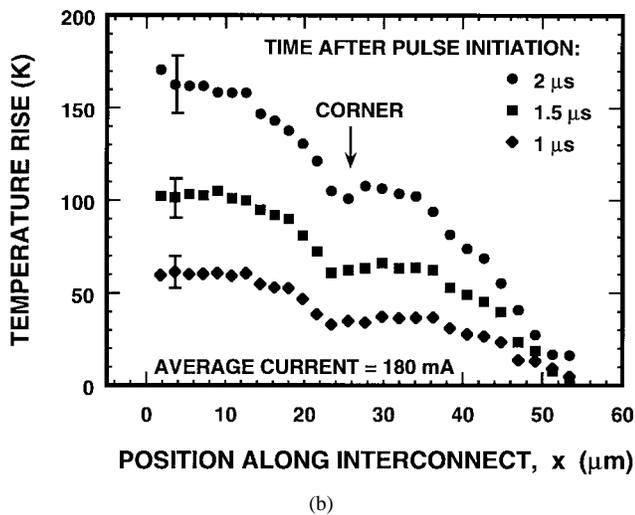
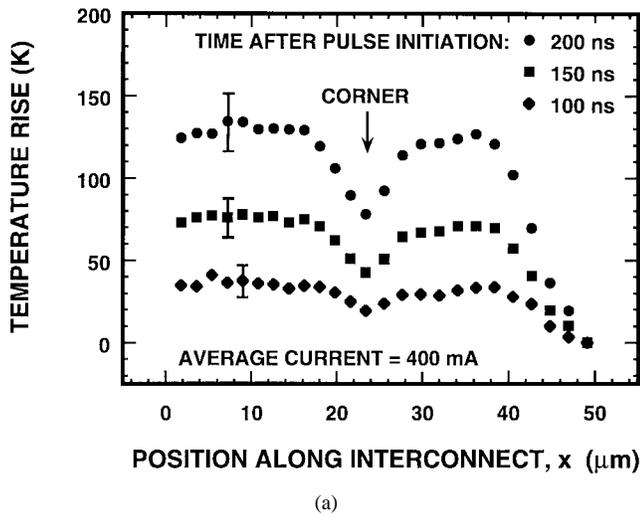


Fig. 3. Transient temperature rise profiles along the centerlines of interconnects with sharp corners subjected to electrical pulses of duration (a) 250 ns and (b) 2.5 μ s.

and more important, which leads to the significant changes in the temperature profiles as illustrated in the figure.

IV. SUMMARY AND CONCLUSIONS

Rapid temperature rises during brief electrical stressing events can lead to failures of interconnects in VLSI circuits. These failures are strongly influenced by spatial variations

in the temperature rise caused by the presence of corners, contacts, vias and neighboring devices or interconnects. In this manuscript, we report transient scanning laser-reflectance thermometry of metal interconnects in VLSI circuits. A two-step calibration procedure for interconnects is also developed that uses the interconnects as temperature-sensing electrical resistance thermometers.

The nonuniform rate of heat generations occurring near contact pads and corners, is shown to influence the temperature distribution within interconnects in a manner sensitive to the duration of stressing pulses. The localized hot spots formed due to nonuniform current distributions are most pronounced for brief pulses.

ACKNOWLEDGMENT

The interconnect samples were provided by Intel Corporation. The authors appreciate helpful discussions with Dr. Amerasekera.

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