Abstract—We report spatial mapping of temperature fields in semiconductor devices with sub-microsecond temporal resolution. The measurements are performed at a facility that integrates scanning laser-reflectance thermometry with electrical stressing capability. Data for SOI LDMOS transistors investigate transient heat diffusion within the buried silicon dioxide and capture large temperature gradients in the drift region, which result from the spatially-varying impurity concentration. The new thermometry facility is promising for the study of transistor and interconnect thermal failure due to electrostatic discharge (ESD).

I. INTRODUCTION

SEMICONDUCTOR devices must withstand short-timescale electrical stressing phenomena, some of which induce severe degradation or failure due to the resulting temperature rise. Electrostatic discharge (ESD), for example, can yield device or interconnect melting during current pulses shorter than 100 ns [1], [2]. Transistors can be designed to better withstand such stressing through thermal design, which relies on accurate simulation capability. But simulation of thermal failure phenomena need transient temperature-field data for verification and improvement of model parameters. Recent research developed techniques for mapping steady-state temperature fields in semiconductor devices [3]–[7], but the technically critical problem of transient thermometry has not received much attention. Transient thermometry of SOI LDMOS transistors was performed by Arnold et al. [8], who used the temperature-dependent bias current to investigate transistor cooling after heating pulses of duration comparable to 1 μs. This method has the advantage that it does not require any modification of devices. But this approach does not yield the spatial variation of temperature within a device. This letter communicates thermal mapping of SOI LDMOS transistors with high temporal and spatial resolution using laser-reflectance thermometry, which detects temperature changes near a surface using the temperature-dependence of optical properties [9]–[13].

II. EXPERIMENTS

Measurements are performed at the facility shown in Fig. 1, which integrates scanning laser diagnostics and electrical probing. Radiation from a laser diode is coupled into an optical microscope and focused to a diameter near the wavelength, 820 nm. A polarization cube and a quarter-wave plate separate the incident and reflected probe beam paths. The radiation powers are captured using photodiodes with 500 MHz bandwidth and a digital oscilloscope with 1 GHz sampling frequency. Laser power fluctuations are subtracted using a reference beam drawn by a beam splitter. The probe laser focus is scanned over the wafer surface using a pair of galvanometrically-actuated mirrors that rotate about orthogonal axes, while the semiconductor device remains stationary.

The technique is applied to SOI LDMOS transistors fabricated using BESOI substrates and the method of Leung et al. [7]. The drift region is 40 μm long and the total device area, including the enclosed drain, is 0.32 mm². The total width of the drift region is 2 mm. To assist with the thermometry, an aluminum layer of thickness 25 nm is sputtered within the surface oxide as shown in Fig. 2. Because the aluminum layer is opaque to radiation at 820 nm, it prevents interaction between the radiation and the transistor and precisely defines the vertical location at which temperature is measured. But
the presence of the aluminum and its separation from the drift region limits the spatial and temporal resolution of the measurements. To reduce the total thickness of the silicon dioxide layer, part of the thermal oxide, shown as a gray region on top of the drift region in Fig. 2, is etched away before the deposition of a CVD oxide layer. The importance of lateral heat conduction within the aluminum layer can be estimated by using the thermal decay length [14],

\[ L_D = (k_\text{al}d_\text{al}/k_\text{ox})^{1/2} \]

where \( k_\text{al} \) and \( d_\text{al} \) are the aluminum thermal conductivity and thickness, respectively, and \( k_\text{ox} \) and \( d_\text{ox} \) are the thermal conductivity and thickness of the oxide separating the aluminum from the device. The thermal decay length is \( \approx 1 \mu\text{m} \), resulting in a spatial resolution limit that is important but not more restrictive than that due to the diffraction of the incident probe laser beam. The spatial resolution limit due to heat spreading within the silicon dioxide layer is comparable to its thickness, 0.6 \( \mu\text{m} \), and is also not more restrictive than that due to the diffraction. The temporal resolution limit due to the silicon dioxide is approximately given by the time required for heat to diffuse normal to the layer,

\[ t_D = L_{\text{ox}}^2/\alpha_{\text{ox}} \]

where \( L_{\text{ox}} \) is the thickness of the oxide layer and \( \alpha_{\text{ox}} \) is the thermal diffusivity of silicon dioxide. The thermal diffusion time is around 0.5 \( \mu\text{s} \) for the LDMOS transistors studied here.

Periodic voltage pulses of duration near 30 \( \mu\text{s} \) and magnitude near 30 V are applied to the drain with a duty cycle less than 0.01. The gate of the power LDMOS transistor is positively biased at 12 V and the source is grounded. The probe laser beam remains at each location long enough to average the transient photodetector signals during a thousand heating periods. The spatial temperature-rise map at any time is extracted from the periodic temperature-rise data at each point. The temperature dependence of the surface reflectance is calibrated in the absence of electrical heating using a thermal chuck. The relative uncertainty in the absolute magnitude of temperature rise is 0.1 K.

The calculated temperature rise agree well with the data. The noise equivalent temperature resolution is about 0.1 K.

III. RESULTS AND DISCUSSION

Fig. 3 shows the temperature distribution measured along the drift region of an SOI LDMOS transistor for varying times after the initiation of the heating pulse. Since the thermal diffusion time normal to the buried silicon dioxide is comparable to 5 \( \mu\text{s} \), the data actually describe transient heat diffusion within the silicon dioxide surrounding the active region. The temperature rise increases with decreasing coordinate \( y \) due to the spatial variation of the phosphorus impurity concentration. A linear increase in the impurity concentration with coordinate \( y \) is targeted by the fabrication process of the LDMOS transistors to improve their voltage-blocking capability [7]. Since the current density does not vary significantly within the drift region, the rate of heat generation is proportional to the local electrical resistivity. The electrical resistivity decreases with increasing impurity concentration, and therefore the volumetric heating rate decreases with increasing \( y \).

Fig. 3 also shows the predictions of a finite-difference solution to the transient, two-dimensional heat equation in the drift region and surrounding silicon dioxide. The simulation uses bulk resistivity data for phosphorus-doped silicon with concentration distribution that is consistent with the fabrication process. The thermal conductivity and heat capacity used for the calculations are 100 W m\(^{-1}\) K\(^{-1}\) and 1.66 × 10\(^6\) J m\(^{-3}\) K\(^{-1}\) for silicon and 1.4 W m\(^{-1}\) K\(^{-1}\) and 1.65 × 10\(^6\) J m\(^{-3}\) K\(^{-1}\) for silicon dioxide, respectively [15]. The simulation assumes that the top boundary condition for the passivation is adiabatic and the bottom boundary condition for the buried silicon dioxide is isothermal. These assumptions are justified by the extremely low convection and radiation heat losses to the ambient air [5] and by the short timescale of the heating pulse, respectively. The shape and time dependence of the calculated temperature rise agree well with the data.

The spatially averaged temperature rise per unit power per unit area of the drift region in the plane of the substrate is
8 × 10^{-7} \text{ K m}^2 \text{ W}^{-1} \) at the time 10 \( \mu \text{s} \) after the initiation of the pulse. While this differs from the similarly normalized transient thermometry data of Arnold et al. [8], we have shown theoretically that this difference can be almost entirely explained by the difference in the interrogated domain and the dimensions of the devices. Remaining differences may be due to the fact that Arnold et al. [8] measured a weighted average of the temperature in the drift region.

Fig. 4 compares the shapes of the transient temperature rises measured using laser-reflectance thermometry for two values of the buried silicon-dioxide thickness. To make the differences in shape as clear as possible, the temperature-rise curves are normalized by their values at 30 \( \mu \text{s} \). The temperature near the source. The scanning laser-reflectance technique described here achieves better temporal resolution

when the radiation interacts with the region whose temperature is to be detected. This has been shown by subsequent work, which has demonstrated temporal resolution of 10 ns for interconnects on polymer passivation layers [16]. This resolution is promising for future failure studies during electrical overstress phenomena such as electrostatic discharge.

IV. CONCLUSIONS

The temperature distributions along the drift region of SOI LDMOS transistors are measured using a laser thermoreflectance technique. The nonhomogeneity of the impurity concentration in the drift region yields a steep increase in temperature near the source. The scanning laser-reflectance technique described here achieves better temporal resolution in the transient one-dimensional heat equation, also shown in the figure, which are hard to distinguish from the experimental data.

REFERENCES