

Microthermal Stage for Electrothermal Characterization of Phase-Change Memory

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Abstract—This letter describes a novel experimental structure that captures the impact of rapid temperature transients and repetitive cycling on the thermal and electrical properties of $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST). The microthermal stage dramatically improves the temporal resolution for heating and enables simultaneous thermal and electrical characterizations. Thermal conductivity measurements show phase transitions of GST accompanied by abrupt changes in electrical resistance. Repetitive cycling with durations down to 100 ns produces melt-quenched amorphous GST with the thermal conductivity 40% lower than that of crystalline GST. Recrystallization increases conductivity but not up to the value achieved by long-timescale bulk annealing. This is potentially because the rapidly recrystallized GST contains more disorder near the interface.

Index Terms— $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST), microthermal stage (MTS), phase-change memory (PCM), thermal conductivity.

I. INTRODUCTION

PHASE-CHANGE memory (PCM) is based on rapid thermally induced phase transitions in $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST) and related compounds. Because the phase change is induced by temperature changes, thermal conduction governs the critical device figures of merit [1], [2]. The thermal conductivity of GST films has been reported for a wide range of thicknesses [2]–[8]. The past work, however, is limited to blanket films in as-deposited conditions or to samples modified using long (> 1 s) heating events. The existing data fall far short of the needs for accurate simulations of PCM devices, in which nanoscale geometries and brief repetitive heating events yield grain structures and phase distributions that differ strongly from those achieved in bulk slow-anneal experiments. The lack of the needed data can be attributed to the use of a conventional macroscopic stage for temperature control. The temperature rise during the melt-quench process exceeds 600 °C within a few tens of nanoseconds, but there has previously been no way to study the impact of this rapid heating on the fundamental

Manuscript received March 4, 2011; revised April 11, 2011; accepted April 11, 2011. Date of publication May 19, 2011; date of current version June 29, 2011. This work was supported in part by Intel Corporation, by the Semiconductor Research Corporation under Contract 2009-VJ-1996, and by the National Science Foundation under Grant CBET-0853350. The review of this letter was arranged by Editor S. Kawamura.

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Digital Object Identifier 10.1109/LED.2011.2144952

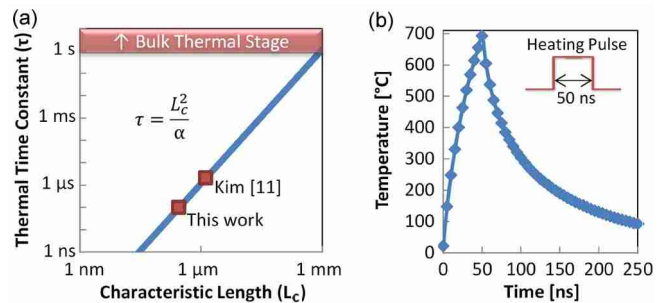


Fig. 1. (a) MTS can reproduce the heating timescales and the temperature excursions of PCM device in the characterization samples. The time constant can be further reduced by decreasing the characteristic length, which is normally defined by thermal passivation layers between GST and the Si substrate. (b) Electrothermal simulation for the experiment used in this letter estimates that the temperature of GST under a 50-ns heating pulse reaches the melting point and then cools down below 300 °C within 50 ns and below 200 °C within 100 ns.

material properties in GST. Rapid temperature transients would enable studies on the impact of medium-range order in melt-quenched GST the potential for higher crystallization rates [9]. Repetitive rapid heating (i.e., cycling with short timescales) is also important because this can reveal the physics behind evolution of the threshold voltage, the reset resistance, and other electrical properties [10].

This letter provides a detailed description of the measurement capabilities of a novel microthermal stage (MTS) that addresses the needs for PCM technology. Fig. 1 shows that the MTS can combine a thermal time constant below 100 ns with heating capability up to 700 °C. Our previous work [11] presented the MTS for the specific study of electrical properties evolution, with relevance for crystallization and drift phenomena in microtimescale. Here, we provide a more comprehensive description of capabilities with a focus on thermal transport. One key benefit of the MTS developed here is that a single structure enables simultaneous characterization of thermal and electrical properties using four-probe electrical-resistance thermometer with a programmable phase-change material (e.g., GST) bridge. This letter reports measurement results including the in-plane electrical resistance and the out-of-plane thermal conductivity during repetitive cycling.

II. EXPERIMENTAL METHODS

A. Design and Fabrication

Samples are prepared on a silicon substrate, which serves as a heat sink for the quenching process. First, a 380-nm-thick thermal oxide (with low thermal conductivity) is grown

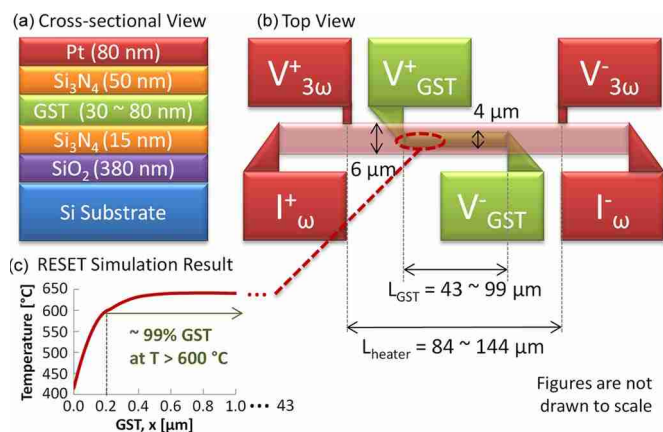


Fig. 2. [(a) and (b)] Schematics of experimental structure for the simultaneous thermal and electrical characterizations. The MTS (image made transparent) covers the entire area of the GST bridge for uniform heating and thermometry. Electrical pulses applied on the GST pads program the bridge like lateral PCM cells. The geometry varies by measurements. (c) Electrothermal simulation for the 80-nm-thick 4- μm -wide 43- μm -long GST bridge confirms that nearly 99% of the GST bridge can melt during the RESET process. (a) Cross-sectional view. (b) Top view. (c) RESET simulation result.

to provide for thermal resistance and temperature rise with modest levels of heat generation. After deposition of a 15-nm-thick Si_3N_4 layer, a GST film (thickness of 30, 50, or 80 nm) is deposited by radio-frequency magnetron sputtering in argon with a pressure of 5 mT at the room temperature. While some samples are prepared with the blanket film for validation, programmable GST bridges are patterned by a dual-layer liftoff. The bridge dimensions [see Fig. 2(b)] are limited by heating power considerations and the resolution of lithography. A 50-nm-thick Si_3N_4 layer is sputtered over GST for electrical passivation. A 80-nm-thick Pt layer is also deposited by sputtering, and MTS structures are patterned by liftoff. All the samples are annealed at 200 °C for 30 min prior to measurements.

B. Programming Conditions

The GST phase strongly depends on programming conditions such as pulse amplitude and time constant. The RESET state develops when the temperature rises above 600 °C and quenches faster than recrystallization. The electrical resistance is monitored while increasing the pulse amplitude. Fig. 3(a) shows the electrical characteristics of GST bridges under programming pulses. The SET state can result from two methods. The first method is to apply electrical pulses directly on the GST bridge until the resistance significantly drops from the RESET state. Fig. 3(b) demonstrates reversible switching between the RESET and SET states using accumulated pulses. The second method is to provide uniform heating over GST using the MTS. After calibrating the temperature coefficient of resistance, the MTS can accurately control the magnitude and the timescale of heating, which recrystallizes amorphous GST.

C. Thermal Conductivity Measurements

The MTS measures the thermal conductivity of GST using the 3ω method. The MTS transmits current at frequency ω and generates Joule heating at 2ω . The resulting change in the

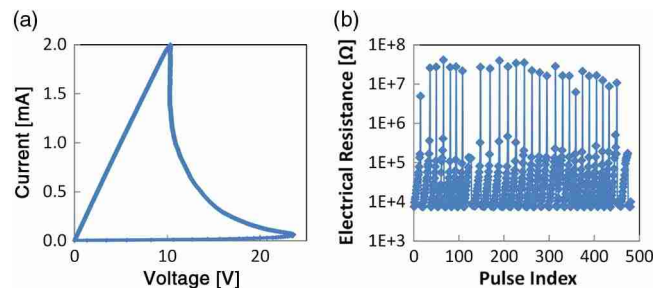


Fig. 3. (a) I - V curve of a 50-nm-thick 2.5- μm -wide 5- μm -long GST bridge demonstrates threshold switching at 23 V, while the RESET pulse of 35 V in 50 ns increases the resistance from 5 k Ω to 1.2 M Ω . (b) The data represents a portion of resistance evolution during repetitive cycling for a 30-nm-thick 2- μm -wide 22- μm -long GST bridge. The RESET resistance variation under constant pulse (17.5 V) might be due to residual crystalline phase.

electrical resistance creates a 3ω component in the voltage. A circuitry of differential amplifiers extracts the 3ω voltage, and a lock-in amplifier (SR830) detects the in-phase signal with high sensitivity. The 3ω voltage captures the amplitude of temperature rise in response of underlying materials [3], [4], [7]. Differential measurements with and without GST determine the temperature drop exclusively across GST by canceling the effects of substrate and passivation layers. The thermal conductivity is measured at every SET and RESET states. Since the exact area of melt-quenched amorphous GST is unknown, electrothermal simulation using a finite-element code (COMSOL) estimates the area fractions based on the temperature distribution. The simulation result [see Fig. 2(c)] shows nearly 99% of the GST bridge can be uniformly heated above 600 °C, partly due to the heat spreading in the oxide layer. The GST regions 0.2 μm from the edges do not reach the melt-quenched state and are neglected for the thermal conductivity calculation. Although a temperature gradient is observed across the GST thickness, the entire cross section is assumed to be melt quenched. This is based on observations of electrical resistance that abruptly increases after applying a number of constant pulses.

III. RESULTS AND DISCUSSION

The data for the blanket GST films validate the thermal conductivity measurement approach using the MTS. The thickness-dependent data, i.e., 0.31, 0.45, and 0.59 $\text{Wm}^{-1}\text{K}^{-1}$ for the 30-, 50-, and 80-nm-thick crystalline GST films, provide the thermal boundary resistance $3.6 \times 10^{-8} \text{ m}^2\text{KW}^{-1}$ and the intrinsic thermal conductivity $1.27 \text{ Wm}^{-1}\text{K}^{-1}$. These data are consistent with our past work [3], [6] and literature values [2]–[8]. The thermal conductivity of blanket films also matches that of GST bridges. The confined geometry has the same value because the thermal conductivity measurements restrict the heat in the out-of-plane direction.

Fig. 4 shows the conductivities of GST subject to rapid phase transitions. Electrical pulses 50 V high in 50 ns applied on the 30-nm-thick 4- μm -wide 99- μm -long GST bridge significantly reduce both conductivities. The thermal conductivity of the melt-quenched GST is 40% lower than bulk annealed crystalline GST and 25% lower recrystallized GST. Melt-quenched GST may contain a small fraction of crystalline

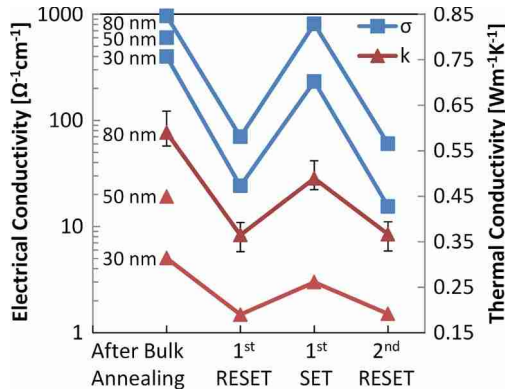


Fig. 4. Electrical and thermal conductivities of GST subject to rapid phase transitions. The RESET pulses applied on the GST produce the melt-quenched amorphous phase. While the 30-nm-thick GST sample recrystallizes by threshold switching, the 80-nm-thick GST sample recrystallizes by MTS annealing. Both recrystallization methods increase conductivity but not up to the value achieved by long-timescale bulk annealing.

phase [12], particularly with long quenching time. Residual crystalline filaments could explain the occasional occurrence of low RESET resistance observed in Fig. 3(b). Compared with the electrical conductivity measurements, the out-of-plane thermal conductivity measurements are less sensitive to the crystalline filaments.

We demonstrate three different formation of crystalline GST including bulk annealing, MTS annealing, and threshold switching. After the first RESET (see Fig. 4), electrical pulses 34 V high in 100 s recrystallize the 30-nm-thick GST sample upon threshold switching. The MTS annealing recrystallizes the 80-nm-thick GST sample with a precisely controlled heating that matches the bulk annealing condition. Both recrystallization methods increase conductivity but only up to 83% of the values achieved by long-timescale bulk annealing. This is potentially because the rapidly recrystallized GST contains more disorder. The temperature gradients in GST, as well as rapid transients during cycling, may induce phase variation and crystal defects near the lower interface. This agrees well with the study of laser-processed GST samples [6], which showed lower thermal conductivity compared with that of long-timescale annealing.

Long GST bridges may increase the measurement sensitivity, but it may also increase the risk of breakdown due to large programming voltages. For example, the 50-nm-thick 4- μm -wide 99- μm -long GST bridge was severely damaged by 60-V RESET pulses after one programming. The durability can be improved without sacrificing the sensitivity by scaling both GST and MTS using advanced lithography. An optimized MTS structure could profile electrical and thermal conductivity evolutions of GST for an extended number of programming cycles.

IV. CONCLUSION

This letter have presented the MTS as a highly versatile platform for thermal and electrical measurements of phase-change material. The thermal conductivity measurements have shown phase transitions of GST, accompanied by abrupt changes in electrical resistance. Repetitive thermal cycling with durations down to 100 ns has produced melt-quenched amorphous GST with the thermal conductivity 40% lower than that of crystalline GST. Recrystallization increased the conductivity but not up to the value achieved by long-timescale bulk annealing. Understanding the impact of repetitive cycling on thermal and electrical properties can improve the device performance and reliability, which are vital for the novel PCM.

REFERENCES

- [1] J. P. Reifenberg, D. L. Kencke, and K. E. Goodson, "The impact of thermal boundary resistance in phase-change memory devices," *IEEE Electron Device Lett.*, vol. 29, no. 10, pp. 1112–1114, Oct. 2008.
- [2] V. Giraud, J. Cluzel, V. Sousa, A. Jacquot, A. Dauscher, B. Lenoir, H. Scherrer, and S. Romer, "Thermal characterization and analysis of phase change random access memory," *J. Appl. Phys.*, vol. 98, no. 1, p. 013520, Jul. 2005.
- [3] J. Lee, Z. Li, J. P. Reifenberg, M. Asheghi, and K. E. Goodson, "Thermal conductivity anisotropy and grain structure of $\text{Ge}_2\text{Sb}_2\text{Te}_5$ films," *J. Appl. Phys.*, vol. 109, no. 8, p. 084 902, Apr. 2011.
- [4] E. K. Kim, S. I. Kwun, S. M. Lee, H. Seo, and J. G. Yoon, "Thermal boundary resistance at $\text{Ge}_2\text{Sb}_2\text{Te}_5/\text{ZnS}:\text{SiO}_2$ interface," *Appl. Phys. Lett.*, vol. 76, no. 26, pp. 3864–3866, Jun. 2000.
- [5] H. K. Lyeo, D. G. Cahill, B. G. Lee, J. R. Abelson, M. H. Kwon, K. B. Kim, S. G. Bishop, and B. K. Cheong, "Thermal conductivity of phase-change material $\text{Ge}_2\text{Sb}_2\text{Te}_5$," *Appl. Phys. Lett.*, vol. 89, no. 15, p. 151 904, Oct. 2006.
- [6] J. P. Reifenberg, M. A. Panzer, S. Kim, A. M. Gibby, Y. Zhang, S. Wong, H.-S. P. Wong, E. Pop, and K. E. Goodson, "Thickness and stoichiometry dependence of the thermal conductivity of GeSbTe films," *Appl. Phys. Lett.*, vol. 91, no. 11, p. 111 904, Sep. 2007.
- [7] W. P. Risk, C. T. Rettner, and S. Raoux, "Thermal conductivities and phase transition temperatures of various phase-change materials measured by the 3ω method," *Appl. Phys. Lett.*, vol. 94, no. 10, p. 101 906, Mar. 2009.
- [8] J.-L. Battaglia, A. Kusiak, V. Schick, A. Cappella, C. Wiemer, M. Longo, and E. Varesi, "Thermal characterization of the $\text{SiO}_2\text{-Ge}_2\text{Sb}_2\text{Te}_5$ interface from room temperature up to 400 °C," *J. Appl. Phys.*, vol. 107, no. 4, p. 044314, Feb. 2010.
- [9] M.-H. Kwon, B.-S. Lee, S. N. Bogle, L. N. Nittala, S. G. Bishop, J. R. Abelson, S. Raoux, B.-k. Cheong, and K.-B. Kim, "Nanoscale order in amorphous $\text{Ge}_2\text{Sb}_2\text{Te}_5$ analyzed by fluctuation electron microscopy," *Appl. Phys. Lett.*, vol. 90, no. 2, p. 021923, Jan. 2007.
- [10] J. Sarkar and B. Gleixner, "Evolution of phase change memory characteristics with operating cycles: Electrical characterization and physical modeling," *Appl. Phys. Lett.*, vol. 91, no. 23, p. 233 506, Dec. 2007.
- [11] S. Kim, B. Lee, M. Asheghi, F. Hurkx, J. P. Reifenberg, K. E. Goodson, and H.-S. P. Wong, "Resistance and threshold switching voltage drift behavior in phase-change memory and their temperature dependence at microsecond time scales studied using a microthermal stage," *IEEE Trans. Electron Devices*, vol. 58, no. 3, pp. 584–592, Mar. 2011.
- [12] M. S. Youm, Y. T. Kim, and M. Y. Sung, "Observation of hexagonal nuclei in the once melt-quenched $\text{Ge}_2\text{Sb}_2\text{Te}_5$ phase change contact dimensions," *Appl. Phys. Lett.*, vol. 91, no. 8, p. 083508, Aug. 2007.