

# Grain Boundaries, Phase Impurities, and Anisotropic Thermal Conduction in Phase-Change Memory

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**Abstract**—Thermal conduction strongly influences the programming energy and speed in phase-change-memory devices. The thermal conductivity of the crystalline phase of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  can be strongly anisotropic due to phase impurities at grain boundaries. This letter models this effect using effective medium arguments, lends further support to the hypothesis that phase impurities are responsible for the anisotropy, and estimates the impact of anisotropic heat conduction on device performance. Electrothermal simulations predict that the reduced in-plane conductivity will allow closer spacing of lateral-cell devices and reduce the reset programming current by 20%–30%.

**Index Terms**—Chalcogenide, nonvolatile memories, phase-change memory (PCM), thermal conductivity anisotropy.

## I. INTRODUCTION

PHASE CHANGE memory (PCM) is promising for next-generation nonvolatile memory applications [1], [2]. PCM uses the difference in electrical resistivity between the crystalline and amorphous phases of chalcogenides such as  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  (GST) [3]. Thermal properties and models are important for predicting programming current and thermal disturbances among neighboring devices [2], [4], [5]. Our recent work reported anisotropic thermal conduction in GST due to amorphous phase impurities in GST films [6], but no available theory rigorously models this effect and the impact on device performance has not been assessed. Electrical conduction modeling is expected to be similar to thermal conduction given the grain structure and phase composition of GST thin films [7]. Understanding the impact of anisotropic thermal conduction is essential for improved PCM engineering and simulation. This letter uses the effective medium theory (EMT) to model the conductivity anisotropy, validates the model using our past experimental data, and predicts the impact of the anisotropy on PCM device design.

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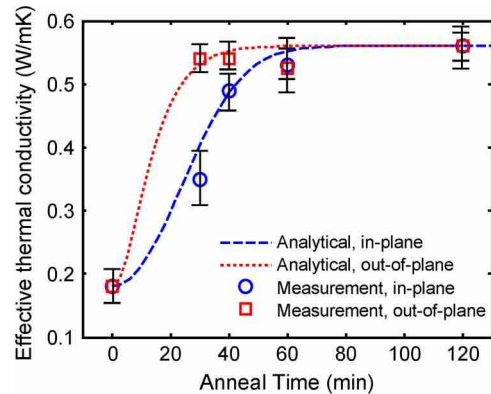


Fig. 1. Data for the in-plane and out-of-plane thermal conductivities of GST films, summarized here based on a full-length paper [6], and compared with the model developed in this paper. The amorphous GST was annealed at 150°C for each time duration.

## II. THERMAL CONDUCTIVITY ANISOTROPY MEASUREMENT

We measured the anisotropic thermal conductivity of GST films using suspended structures and varying width heaters that are sensitive to anisotropy. A radio-frequency magnetron sputtering system deposited GST films with thickness of 200–400 nm. Experimental details are documented in [6] and [8]. Fig. 1 shows that the phase impurity affects the effective thermal conductivity of GST thin films.

Varying the duration of annealing achieves different levels of crystallization. The overall volume fraction of the crystalline phase  $p_c$  depends on the annealing temperature and duration. For an isothermal phase transformation,  $p_c$  can be predicted using the Johnson–Mehl–Avrami–Kolmogorov (JMAK) equation [9]

$$p_c = 1 - \exp(-Kt^m) \quad (1)$$

where  $t$  is the annealing time,  $m$  is the Avrami exponent, and  $K$  is a rate constant. The Avrami exponent, which depends on the type of nucleation and the crystal growth morphology, is set to two for the GST films assuming interface-controlled 1-D growth nucleation at a constant rate [10]. The rate constant is determined from the best fit to the data.

The amorphous GST film has an isotropic thermal conductivity. In-plane and out-of-plane thermal conductivities deviate from each other during the GST crystallization process. Because an annealing duration of more than 60 min at 110°C completely crystallizes the GST film, the thermal conductivity anisotropy disappears. The next section presents a way to

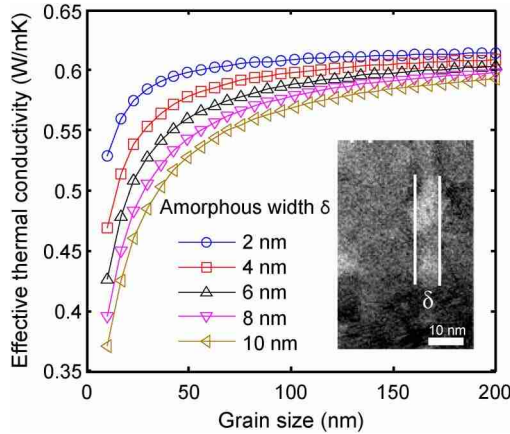


Fig. 2. Calculated effective thermal conductivities of f-GST as a function of grain size. The extent of the amorphous region ( $\delta$ ) between crystalline grains is estimated from TEM image [6].

describe the anisotropic grain formation, which, when combined with the JMAK equation, models the thermal conductivity anisotropy in the GST films.

### III. MODELING THE ANISOTROPY

GST with a crystalline–amorphous mixture can be treated as a heterogeneous material with two phases. This letter models the thermal conductivity of GST films using the Maxwell–Eucken (M-E) theory [11]–[13], which is a derivative of the EMT [14]. Assuming that one of the two phases is continuous while the other is dispersed, the M-E theory describes the thermal and electrical conductivities of binary mixtures. Our previous work [6] demonstrated the columnar growth of crystalline grains normal to the surface for GST films annealed at 150°C for 30 min using transmission electron microscopy (TEM). This past work [6] also identified amorphous regions of characteristic dimension  $\sim 6$  nm located within the continuous crystalline phase at grain boundaries, as shown in the inset of Fig. 2. Grains tend to grow from the film boundaries and elongate vertically with amorphous residues located at grain boundaries [6], [8]. These amorphous regions may originate from incomplete crystal nucleation and growth. Because the grain size of the crystalline GST film is significantly larger than the phonon mean free path of 1 nm in GST [6], [15], the effect of phonon scattering at grain boundaries is neglected.

For the crystalline-amorphous GST film modeled here, the thermal conductivity is predicted using the M-E theory as

$$K_{\nu} = \frac{k_c p_{c,\nu} + 3k_c k_a (1 - p_{c,\nu}) / (2k_c + k_a)}{p_{c,\nu} + 3k_c (1 - p_{c,\nu}) / (2k_c + k_a)} \quad (2)$$

where  $K_{\nu}$  is the effective thermal conductivity in direction  $\nu$  (in plane or out of plane).  $k_c$  and  $k_a$  are the thermal conductivities of pure crystalline and amorphous GST films, respectively. The volume fraction of the crystalline phase can be estimated as  $p_{c,\nu} = d_{g,\nu} / (d_{g,\nu} + \delta)$ , where  $\delta$  is the width of amorphous region and  $d_{g,\nu}$  denotes the average grain size in direction  $\nu$ . Fig. 2 shows the effective thermal conductivity calculated as a function of grain size and amorphous region size using (2). The thermal conductivity generally decreases with reducing grain size and increasing volume fraction of amorphous phase.

The vertically aligned elongated grain structure explains the anisotropic heat conduction in GST films. Because the average grain size is much larger in the out-of-plane direction, the volume fraction of the amorphous phase is significantly lower in this direction than in the in-plane direction. Since the thermal conductivity of the amorphous phase is only  $\sim 30\%$  of that of the crystalline phase, the alignment of amorphous inclusions along the vertically oriented grain boundaries results in a higher thermal conductivity in the out-of-plane direction according to the M-E theory. This effect is calculated using (1) and (2) and is illustrated as analytical curves in Fig. 1.

The film thickness may affect the thermal conductivity anisotropy due to geometrically limited grain growth in the out-of-plane direction, particularly when the thickness becomes comparable to the GST grain size. Laterally confined geometry, such as that in confined PCM cells [4], is expected to change the thermal conductivity anisotropy due to the additional interfaces between GST and its surrounding materials. Grain structure will also be strongly influenced by deposition conditions, which may eventually be adjusted to tailor the anisotropic thermal properties of GST in the crystalline phase.

### IV. ANISOTROPY AND DEVICE DESIGN

We simulated a set-to-reset transition for various combinations of the experimentally observed thermal conductivity anisotropy and GST layer thickness. The simulation assumes that the GST volume begins in the crystalline phase and that the entire molten region quenches into the amorphous phase. The simulation also neglects the possible cyclic effect on the material properties. Since thermal boundary resistance (TBR) influences the temperature distribution, we include a typical TBR of 20 m<sup>2</sup>K/GW between the GST layer and electrode [16].

The high temperature during a reset operation of a PCM cell presents a reliability issue by disturbing the state of its neighboring cells [16]. This thermal disturbance limits the minimum cell spacing in PCM arrays. For a given GST thickness, a lower in-plane thermal conductivity confines the heat within the region above the bottom contact more effectively. Fig. 3 shows the comparison of the temperature distributions between the isotropic and the anisotropic heat conduction. For a 100-nm GST layer under this configuration, the minimum cell space is approximately 135 nm for isotropic GST layer to withstand thermal disturbance, while an anisotropy ratio of 0.6 reduces the minimum cell spacing down to around 80 nm. Therefore, anisotropic GST layers offer one route to higher data storage density and decreased risk of thermal disturbance.

Thermal conductivity anisotropy also influences the thermal resistance in a PCM cell, which determines the programming current. We investigate two types of PCM cells: vertical “mushroom” cells, as described in [1], and lateral cells such as those presented in [18]. Fig. 4(a) shows that the programming current for a vertical cell decreases with increasing GST layer thickness due to higher thermal resistance. In addition, for each GST thickness, the programming current is further reduced with smaller thermal conductivity anisotropy ratio ( $\eta = k_x/k_z$ ). The performance of vertical PCM devices also depends on the geometry in specific cell structures. The confined cell in [4], for example, can affect the anisotropy ratio when the lateral

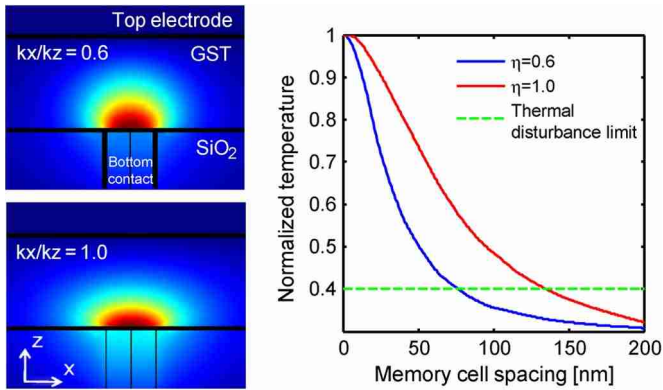


Fig. 3. Electrothermal simulation results. (a) Temperature distribution during reset operation of a PCM cell with anisotropic and isotropic GST layers of 100 nm. (b) Normalized temperature profile along the GST layer in the  $x$  direction. Thermal disturbance limit is set close to the phase transition temperature neglecting cyclic effects.

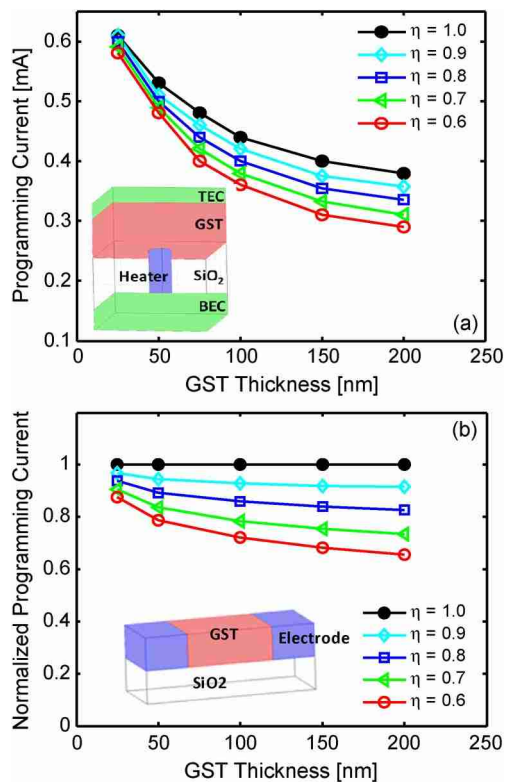


Fig. 4. Programming current during a reset operation as a function of GST film thickness and thermal conductivity anisotropy. (a) Programming current of a vertical PCM cell. (Inset) Schematic of the vertical cell, including bottom electrode contact (BEC) and top electrode contact (TEC) used for simulation. (b) Programming current of a lateral line-shaped cell. (Inset) Lateral cell used in the simulation.

dimensions approach the GST grain size ( $\sim 20$  nm), causing the programming current to deviate from the values predicted here.

The lateral-cell model used in this study is shown in Fig. 4(b). Electrical current flows laterally from one electrode to another, causing Joule heating in the GST bridge that switches the memory cell. Because the cross-sectional area for current flow changes with GST film thickness, we normalize the programming currents to their values under the isotropic heat conduction condition to highlight their relative variation. Fig. 4(b)

shows that, when anisotropy is introduced in the GST layer, the programming current decreases significantly due to the enhanced lateral thermal confinement. An anisotropy ratio  $\eta = 0.6$  reduces the programming current by about 30% for a lateral cell with 100-nm GST layer.

## V. CONCLUSION

This letter has developed a model based on the M-E theory to accurately model the thermal conductivity anisotropy in crystalline GST thin films for PCM. This model relates the directional effective thermal conductivity of GST films to its grain structure and phase purity and is validated by measurement results. Significant reduction of cell spacing and programming current of PCM devices can be achieved considering the anisotropy in the GST layer.

## REFERENCES

- [1] A. L. Lacaita, "Phase change memories: State-of-the-art, challenges and perspectives," *Solid State Electron.*, vol. 50, no. 1, pp. 24–31, Jan. 2006.
- [2] H.-S. P. Wong, S. Raoux, S. Kim, J. Liang, J. P. Reifenberg, B. Rajendran, M. Asheghi, and K. E. Goodson, "Phase change memory," *Proc. IEEE*, vol. 98, no. 12, pp. 2201–2227, Dec. 2010.
- [3] S. Lai, "Current status of the phase change memory and its future," in *IEDM Tech. Dig.*, Dec. 2003, pp. 255–258.
- [4] J. P. Reifenberg, D. L. Kencke, and K. E. Goodson, "The impact of thermal boundary resistance in phase-change memory devices," *IEEE Electron Device Lett.*, vol. 29, no. 10, pp. 1112–1114, Oct. 2008.
- [5] D. L. Kencke, I. V. Karpov, B. G. Johnson, S. J. Lee, D. Kau, S. J. Hudgens, J. P. Reifenberg, S. D. Savransky, J. Zhang, M. D. Giles, and G. Spadini, "The role of interfaces in damascene phase-change memory," in *IEDM Tech. Dig.*, 2007, pp. 323–326.
- [6] J. Lee, Z. Li, J. P. Reifenberg, S. Lee, R. Sinclair, M. Asheghi, and K. E. Goodson, "Thermal conductivity anisotropy and grain structure in  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  films," *J. Appl. Phys.*, vol. 109, no. 8, p. 084902, Apr. 2011.
- [7] J. P. Troadec, D. Bideau, and E. Guyon, "Transport properties of conducting and semiconducting anisotropic mixtures," *J. Phys. C, Solid State Phys.*, vol. 14, no. 32, pp. 4807–4819, Nov. 1981.
- [8] Z. Li, J. Lee, J. P. Reifenberg, M. Asheghi, H.-S. P. Wong, and K. E. Goodson, "In-plane thermal conduction and conductivity anisotropy in  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  films for phase change memory," in *Proc. ASME IMECE*, Nov. 2010, pp. 40459.1–40459.8.
- [9] T. H. Jeong, M. R. Kim, H. Seo, S. J. Kim, and S. Y. Kim, "Crystallization behavior of sputter-deposited amorphous  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  thin films," *J. Appl. Phys.*, vol. 86, no. 2, pp. 774–778, Jul. 1999.
- [10] S. Lombardo, E. Rimini, M. G. Grimaldi, and S. Privitera, "Amorphous-FCC transition in  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ ," *Microelectron. Eng.*, vol. 87, no. 3, pp. 294–300, Mar. 2010.
- [11] A. D. Brailsford and K. G. Major, "The thermal conductivity of aggregates of several phases, including porous materials," *Brit. J. Appl. Phys.*, vol. 15, no. 3, pp. 313–319, Mar. 1964.
- [12] J. C. Maxwell, *A Treatise on Electricity and Magnetism*, 3rd ed. New York: Dover, 1954.
- [13] J. Wang, J. K. Carson, M. F. North, and D. J. Cleland, "A new approach to modeling the effective thermal conductivity of heterogeneous materials," *Int. J. Heat Mass Transf.*, vol. 49, no. 17/18, pp. 3075–3083, Aug. 2006.
- [14] J. Bernasconi, "Conduction in anisotropic disordered systems: Effective-medium theory," *Phys. Rev. B, Condens. Matter*, vol. 9, no. 10, pp. 4575–4579, May 1974.
- [15] H.-K. Lyoo, D. G. Cahill, B.-S. Lee, J. R. Abelson, M.-H. Kwon, K.-B. Kim, S. G. Bishop, and B.-K. Cheong, "Thermal conductivity of phase-change material  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ ," *Appl. Phys. Lett.*, vol. 89, no. 15, p. 151904, Oct. 2006.
- [16] J. P. Reifenberg, K.-W. Chang, M. A. Panzer, S. Kim, J. A. Rowlette, M. Asheghi, H.-S. P. Wong, and K. E. Goodson, "Thermal boundary resistance measurements for phase-change memory devices," *IEEE Electron Device Lett.*, vol. 31, no. 1, pp. 56–58, Jan. 2010.
- [17] A. Pirovano, A. L. Lacaita, A. Benvenuti, F. Pellizzer, S. Hudgens, and R. Bez, "Scaling analysis of phase-change memory technology," in *IEDM Tech. Dig.*, 2003, pp. 699–702.
- [18] M. Lankhorst, B. Ketelaars, and R. Wolters, "Low-cost and nanoscale non-volatile memory concept for future silicon chips," *Nat. Mater.*, vol. 4, no. 4, pp. 347–352, Apr. 2005.