

# Thermal conduction in metallized silicon-dioxide layers on silicon

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The vertical thermal conductivities of thermally grown (TG) and chemical vapor deposited (CVD) silicon-dioxide layers 20 to 200 nm thick are measured using a simple, noncontact photothermal technique. The conductivities of TG and CVD layers are less by as much as 18% and 30%, respectively, than the conductivity of bulk fused silicon dioxide. No significant thickness dependence is observed. The thermal boundary resistance between the oxide layers and silicon is shown to be negligibly small. The boundary resistance of gold layers sputtered directly onto TG oxide is considerably larger than that of gold layers evaporated on TG oxide with a 20-nm chromium adhesion layer, and is comparable to internal resistances of the oxide layers.

Thermal conduction cooling in silicon-based electronic circuits can be limited by silicon-dioxide layers, which have very low internal thermal conductivities.<sup>1</sup> This problem is augmented by thermal resistances at the boundaries of these layers with metal interconnects and with silicon, which reduce the effective conductivity for conduction normal to the silicon dioxide. The thermal-conduction data, that are available for thin silicon-dioxide layers, show a strong dependence of internal conductivities and boundary resistances on the methods used to fabricate the layers.<sup>2</sup> The large variation is not understood and may be due in part to measurement uncertainties. The most accurate measurement techniques use electrical conduction in narrow metal bridges for heat generation or thermometry. The internal silicon-dioxide conductivity must then be separated from thermal resistances near the boundaries of the metal coatings, whose thermal properties are often not known. This work presents thermal-conduction data for thermally grown (TG) and chemical vapor deposited (CVD) silicon-dioxide layers with thicknesses between approximately 10 and 200 nm, which were metallized with gold. The new measurement technique is simple, noncontact, and requires little sample preparation.

Undoped silicon-dioxide layers were grown by thermal oxidation at 850 °C and plasma-enhanced CVD at 300 °C using a mixture of SiH<sub>4</sub> and O<sub>2</sub>. One set of the TG layers was sputtered with 2 μm gold; another set and the CVD layers were evaporated with 20 nm chromium and 2 μm gold. Transient vertical heat flux was generated by surface absorption of a Nd:YAG-laser beam with 6-ns pulse length and Gaussian profile in space, as shown in Fig. 1. The relaxation of the surface temperature, which is strongly influenced by local thermal resistances below the surface, was probed using the thermoreflectance technique. Temperature-induced changes in the reflectivity were monitored by detection of the reflected light of a continuous wave helium-neon laser. The advantage of this technique over common steady-state techniques is the ability to measure without calibrations. The

thermal resistance is deduced from the shape of the temperature response without knowledge of the amplitude.

The transient surface temperature is calculated by solving the one-dimensional heat-conduction equation using the following simplifications:

(i) For thickness  $d \ll 1 \mu\text{m}$ , the propagation time of heat in the SiO<sub>2</sub> films,  $t \approx d^2/\kappa_{\text{SiO}_2}$  (with  $\kappa = k/c$  being the thermal diffusivity, which is the thermal conductivity divided by the heat capacity per unit volume), is more than one magnitude shorter than the time scale of the present measurements,  $t \sim 1 \mu\text{s}$ . Thus the heat capacitance of the SiO<sub>2</sub> film can be neglected and the film is modeled as a thermal resistance,  $R_{\text{th}}$ , without vertical extension between the metal and silicon at the depth  $L$ .

(ii) The silicon substrate is more than one magnitude thicker than the conduction penetration depth. It is modeled as a semi-infinite medium.

(iii) Heat flux at the surface is generated by absorption of the laser light of power density per unit area,  $Q$ . The absorption length is small compared to the conduction penetration depth during the laser pulse, whose duration is much shorter than measurement time scales.

The surface temperature in the frequency domain assumes heat generation with angular frequency  $\omega$ ,

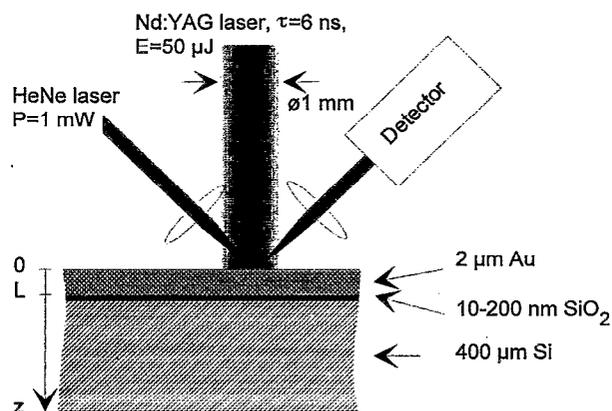


FIG. 1. Experimental geometry for thermoreflectance measurements.

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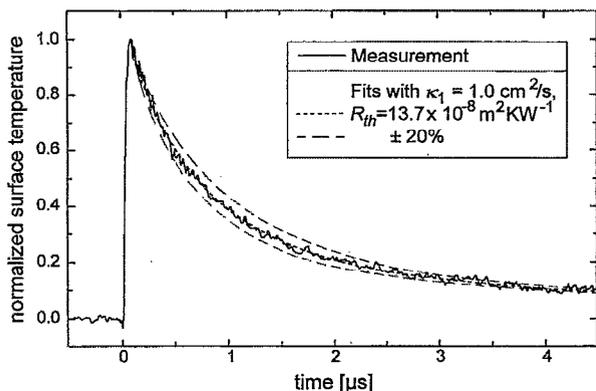


FIG. 2. Transient surface temperature of a CVD silicon-dioxide layer 98 nm thick, coated with 20 nm Cr and 2.0  $\mu\text{m}$  Au. Continuous line: measurement. Dotted line: best fit with Eq. (1). Dashed lines: same parameters, but  $\pm 20\%$  variation of the thermal resistance,  $R_{\text{th}}$ .

$$T(z=0, \omega) = \frac{Q}{k_1 \beta_1} \frac{\chi(1 + e^{-2\beta_1 L}) + 2\eta}{\chi(1 - e^{-2\beta_1 L}) + 2\eta} e^{i\omega t + \text{c.c.}}, \quad (1)$$

where

$$\beta_1 = \sqrt{\frac{i\omega}{\kappa_1}}, \quad \beta_2 = \sqrt{\frac{i\omega}{\kappa_2}}, \quad \eta = \frac{k_2 \beta_2}{k_1 \beta_1},$$

$$\chi = 1 + k_2 \beta_2 R_{\text{th}} - \eta$$

and with indices “1” for the metallic layer and “2” for the silicon substrate. The transient temperature response  $T(z=0, t)$  to the laser pulse is obtained by numerical Fourier transformation of Eq. (1).

Figure 2 shows an example of a measured surface temperature rise, normalized by its maximum value of roughly 10 K. The fits use thermal-conductivity and specific-heat data of the substrate,  $k=1.45 \text{ W cm}^{-1} \text{ K}^{-1}$  and  $c=1.65 \text{ J cm}^{-3} \text{ K}^{-1}$ , specific-heat data of the gold film,  $c=2.49 \text{ J cm}^{-3} \text{ K}^{-1}$ , and the measured gold film thickness,  $L=2.0 \mu\text{m}$ . The vertical thermal diffusivity of the gold film and the thermal resistance due to the silicon dioxide are the only free parameters of the fits.

Figure 3 shows the measured thermal resistances of the TG and CVD silicon dioxide layers as a function of layer thickness. In addition, the thermal resistance of the natural oxide on a silicon wafer was measured. The oxide layer thicknesses are measured using ellipsometry with an error of less than  $\pm 5\%$ . The thickness of the natural oxide was estimated with poorer accuracy. The gold film diffusivity  $\kappa_1$ , averaged over the film thickness, was found to be  $1.0 \text{ cm}^2/\text{s} \pm 20\%$  for the evaporated films, and  $0.8 \text{ cm}^2/\text{s} \pm 20\%$  for the sputtered layers. Both values are significantly smaller than the literature bulk value of  $1.28 \text{ cm}^2/\text{s}$ . The errors were estimated from the quality of the fits, the reproducibility of measurements and the uncertainties in the input parameters.

An increase of the thermal resistance with layer thickness is observed for both TG and CVD silicon-dioxide layers. The linear slopes for the TG layers with different metallizations are very similar, but have different offset values when extrapolated to zero layer thickness. The slope of the

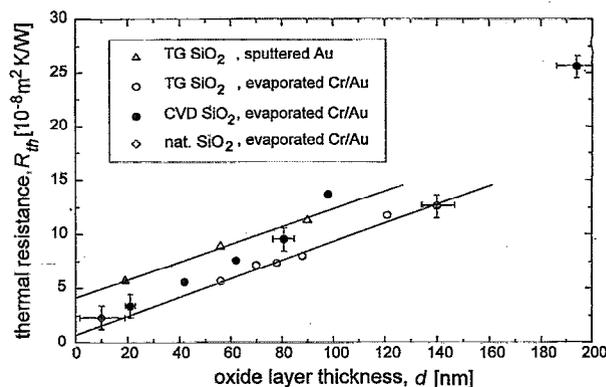


FIG. 3. Thermal resistance data for metallized oxide layers. The lines are linear regressions of the TG layer data.

CVD layers is significantly larger but the offset thermal resistance is approximately the same as that of the TG layers with identical metallization.

The measured thermal resistance,  $R_{\text{th}}$ , is assumed to consist of a volume resistance internal to the oxide layer,  $d/k_{\text{int}}$ , and boundary resistances between the silicon dioxide and the silicon,  $R_{B1}$ , and between the silicon dioxide and the metal,  $R_{B2}$ , yielding

$$R_{\text{th}}(d) = d/k_{\text{int}}(d) + R_{B1} + R_{B2}. \quad (2)$$

Room-temperature thermal boundary resistances between metals and dielectrics are between  $10^{-8}$  and  $10^{-7} \text{ m}^2 \text{ K W}^{-1}$ .<sup>3</sup> This is explained by imperfections at the interface, e.g., regions of incomplete contact, and close to the interface, e.g., dislocations, cracks, porosity, and impurities, as reviewed by Lambropoulos *et al.*<sup>4</sup> The boundary resistance due to acoustic mismatch is more than one magnitude smaller, and therefore negligible.<sup>3</sup>

Imperfections in the silicon-dioxide layer are considered in the volume resistance,  $d/k_{\text{int}}(d)$ . The adhesion and microstructure of the metal, and therefore the silicon/metal resistance,  $R_{B2}$ , is assumed to be independent of the sort and thickness of silicon dioxide below it. The silicon/oxide resistance,  $R_{B1}$ , may be due to incomplete adhesion of the oxide layer or due to a thin interfacial layer with unusually low thermal conductivity.<sup>5</sup> For interfacial layer thicknesses much smaller than those of the investigated oxide layers, this resistance can be modeled as thickness-independent boundary resistance.

The linear extrapolation to zero silicon-dioxide layer thickness yields  $R_{\text{th}}=0.8 \times 10^{-8} \text{ m}^2 \text{ K W}^{-1}$  for the evaporated gold/chromium films and  $R_{\text{th}}=4.3 \times 10^{-8} \text{ m}^2 \text{ K W}^{-1}$  for the sputtered gold films without interfacial chromium layer, both deposited on TG silicon dioxide. Based on the observed improvement of adhesion obtained by using a chromium interfacial layer, it is plausible that regions of incomplete contact are responsible for significant thermal resistances in the layers without chromium. The small difference in the thermal resistance of the thinnest TG and CVD silicon dioxide layers, which were metallized by the same process, suggest that the thermal boundary resistance is caused by the metal/oxide

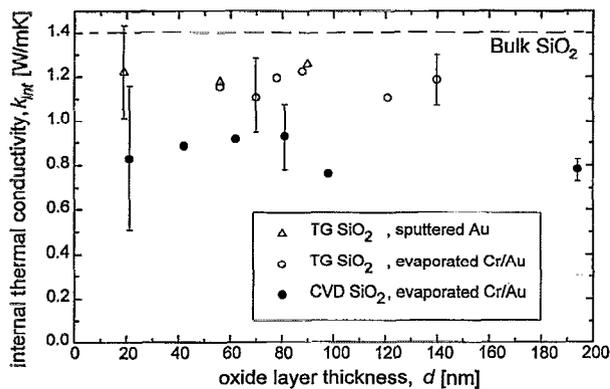


FIG. 4. Internal thermal conductivities of silicon-dioxide layers,  $k_{int}$ . Symbols correspond to Fig. 3.

interface rather than by the silicon-dioxide/silicon interface, whose resistance must be less than  $R_{th} = 0.8 \times 10^{-8} \text{ m}^2 \text{ K W}^{-1}$  for both sets of oxide.

Once having fixed the thickness-independent thermal resistances, the values of the internal thermal conductivities of the silicon dioxide layers, shown in Fig. 4, can be deduced from Fig. 3 by using Eq. (2). The boundary resistances of the CVD layers were assumed to be the same as for the TG layers metallized by the same process. The internal thermal conductivity values for the TG oxide layers do not depend on film thickness and are less than the literature bulk value of fused silica  $k = 1.4 \text{ W/mK}$  and comparable to the values of low-pressure CVD silicon dioxide, annealed near  $750 \text{ }^\circ\text{C}$ .<sup>6</sup> The internal thermal conductivities of the present CVD layers are considerably lower than those of the TG layers and are about 70% of the literature value without a significant thickness dependence.

The data show that the TG layers must have a significant amount of defects. Because of the rather slow, high-temperature oxidation process, the layers are probably free of porosity and cracks and should have good contact to the silicon substrate. The lower conductivity may be related to impurities in the silicon dioxide. The growth of the CVD layers at much lower temperatures can lead to structural disorder. The values reported here are in contrast to previously reported values for plasma-enhanced CVD layers, which were orders of magnitude less than bulk values and decreased rapidly with decreasing layer thickness.<sup>5</sup>

In summary, the thermal conductivity of silicon-dioxide layers on silicon substrates 20 to 200 nm thick is considerably less than the bulk value, and is not thickness dependent. This does not confirm a large variation with film thickness of structural disorder. No significant thermal boundary resistance between silicon dioxide and the substrate was found. In contrast, thermal boundary resistances between silicon dioxide and the metallic coatings near the interface are strongly dependent on the fabrication process and are comparable to internal resistances of the oxide layers.

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<sup>1</sup>L. J. McDaid, S. Hall, P. H. Mellor, W. Eccleston, and J. C. Alderman, *Electron. Lett.* **25**, 827 (1989).

<sup>2</sup>K. E. Goodson and M. I. Flik, *Thermal Sci. Eng.* **2**, 191 (1993), and references therein.

<sup>3</sup>E. T. Swartz and R. O. Pohl, *Appl. Phys. Lett.* **51**, 2200 (1987).

<sup>4</sup>J. C. Lambropoulos, S. D. Jacobs, S. J. Burns, L. Shaw-Klein, and S.-S. Hwang, in *Thin Film Heat Transfer—Properties and Processing*, edited by M. K. Alam, M. I. Flik, G. P. Grigoropoulos, J. A. C. Humphrey, R. L. Mahajan, and V. Prasad (ASME, New York, 1991), p. 21.

<sup>5</sup>F. R. Brotzen, P. J. Loos, and D. P. Brady, *Thin Solid Films* **207**, 197 (1992).

<sup>6</sup>K. E. Goodson, M. I. Flik, L. T. Su, and D. A. Antoniadis, *IEEE Electron Devices Lett.* **14**, 490 (1993).