The Impact of Thermal Boundary Resistance in Phase-Change Memory Devices

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***Abstract*—Thermal conduction governs the writing time and energy of phase-change memory (PCM) devices. Recent measurements demonstrated large thermal resistances at the interfaces of phase-change materials with neighboring electrode and passivation materials. In this letter, electrothermal simulations quantify the impact of these resistances on the set to reset transition. The programming current decreases strongly with increasing boundary resistance due to increased lateral temperature uniformity, which cannot be captured using a reduced effective conductivity in the phase-change material. Reductions in programming current from 20% to 30% occur for an interface resistance of 50 $m^2 \cdot$ K/GW. The precise spatial distribution of thermal properties is critical for the simulation of PCM devices.**

***Index Terms*—Design automation, nonvolatile memories, phase-change memory (PCM), thermal boundary resistance.**

I. Introduction

PHASE-CHANGE memory (PCM) promises reduced read/write times and improved scalability and endurance compared with Flash technology [1]–[3]. PCM performance benchmarks, including the programming current, depend strongly on material properties and device geometry [4]–[8]. Thermal properties and models are particularly important for predicting programming current [8], threshold voltage [9], and R-I behavior [9]. Thermal boundary resistance is partly responsible for the strong size dependence of the effective thermal conductivity of GeSbTe layers [10]. Kencke *et al.* [8] showed the combined effects of thermal and electrical boundary resistances on reducing programming current, but no work has isolated the impact of the thermal boundary resistance. This letter focuses specifically on the impact of this boundary resistance in devices and predicts strong influences on the device temperature profile and programming current.

II. Thermal Boundary Resistance

No broadly accepted model currently exists for predicting TBR at temperatures above tens of kelvins [11], [12]. The acoustic mismatch (AM) and diffuse mismatch (DM) models lend insight into the source of TBR as partial transmission of energy carriers. More recent lattice dynamical (LD) models capture important interface physics neglected by the continuum AM and DM approaches. LD models capture the impact of interface disorder, lattice mismatch, interface bond strengths, and phonon dispersion at high frequencies on the phonon transmission coefficient [13]–[15], but they require precise information about atomic arrangements that is unavailable for PCM interfaces. The thermal boundary resistance between a broad variety of materials ranges from 1 to 100 $m^2 \cdot$ K/GW at room temperature [16], [17]. Room temperature measurements of the TBR between phase-change material $Ge_2Sb_2Te_5$ (GST) and materials of interest vary from 5 to over 30 $m^2 \cdot$ K/GW [18], [19]. LD calculations on Lennard–Jones (LJ) solids predict that the TBR decreases linearly with temperature by $\sim$11% per 100 K for an LJ solid melting at 900 K [16]. At the upper bound, TBR at the GST–bottom contact (BC) interface would approximately double the thermal resistance of a 50-nm GST layer. This letter varies the GST TBR from 0 $m^2 \cdot$ K/GW (i.e., perfect thermal interface) to 100 $m^2 \cdot$ K/GW.

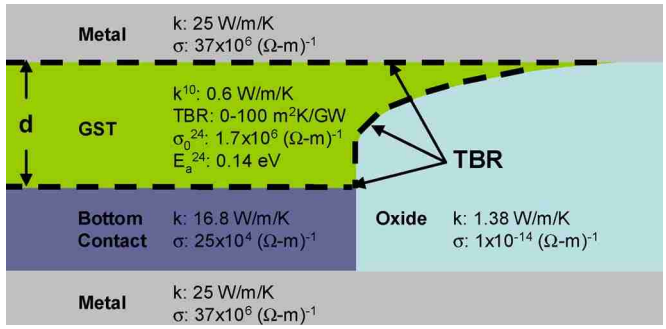

Fig. 1. Schematic of the model geometry, including electrical and thermal properties. The dashed lines indicate the interfaces where the TBR is applied. The model is axially symmetric about the left boundary.

III. Electrothermal Modeling and Implementation

Fig. 1 shows the GST phase-change cell geometry used here. Other PCM geometries include the planar and edge-contact cells [20]. Device geometry affects programming current by changing thermal confinement [20], [21]. TBR can significantly enhance confinement and should be considered in geometries where the TBR is comparable to bulk thermal resistances in series with the interfaces.

The temperature profile is determined by the steady-state heat diffusion equation with Joule heating. The GST interface condition considers the TBR using $q'' = \Delta T / R_{\mathrm{th}}$, where q'',

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ΔT, and $R_{\rm th}$ are the heat flux, the temperature drop across the boundary, and the TBR, respectively. The TBR is uniform at all GST interfaces, although this is unlikely in actual devices. Joule heating and temperature-dependent electrical conductivity couple the heat equation to the Poisson equation for the electrical potential and current distributions. Transient simulations approach the steady-state solution after $\sim$1 ns because programming pulses are much longer [3] than the thermal time constant [22].

Fig. 1 shows the thermal and electrical conductivities used in the simulations. Data show that the FCC phase thermal conductivity increases with temperature up to $\sim$300 °C with a slope of $\sim$0.0025 W/m/K^2 above 200 °C [10], [23]. Our work assumes constant thermal conductivity since no data are available at temperatures above 300 °C. We neglect the temperature dependence of TBR. Both assumptions cause the model to overpredict the total thermal resistance and underestimate the programming current. The ratio of the two resistances is not strongly affected since both resistances are expected to decrease in similar proportion to their room temperature values. The temperature dependence of the electrical conductivity of crystalline GST follows that of a semiconductor [24], namely, $\sigma = \sigma_0 \exp(-E_a/k_bT)$, where E_a is an electrical activation energy and k_b is the Boltzmann constant.

We simulated a set to reset transitions for various TBR and GST thickness combinations and for different effective thermal conductivities with no TBR. Fig. 1 shows the simulation geometry with GST thickness d, a confinement depth of 25 nm, and a BC contact diameter (CD) of 50 nm with height of 150 nm. The minimum current required to transition the cell from high to low resistance (set to reset states) defines the programming current. The simulations assume that the GST volume begins in the crystalline phase and that the entire molten region quenches into the amorphous phase.

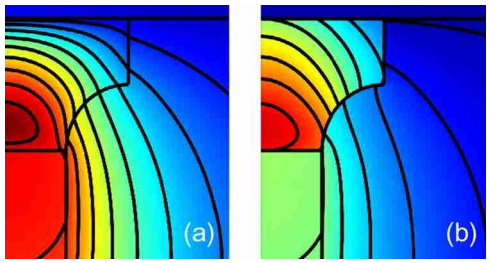

Fig. 2. Temperature profiles for reset simulations with GST thickness of 50 nm. (a) No TBR is applied between the GST interfaces. (b) Result of a TBR of 50 m^2 · K/GW. The temperature scale is the same in each figure. The peak temperature in (a) is 1092 K with a programming current of 1.6 mA, and the peak temperature in (b) is 1015 K with a programming current of 1.2 mA.

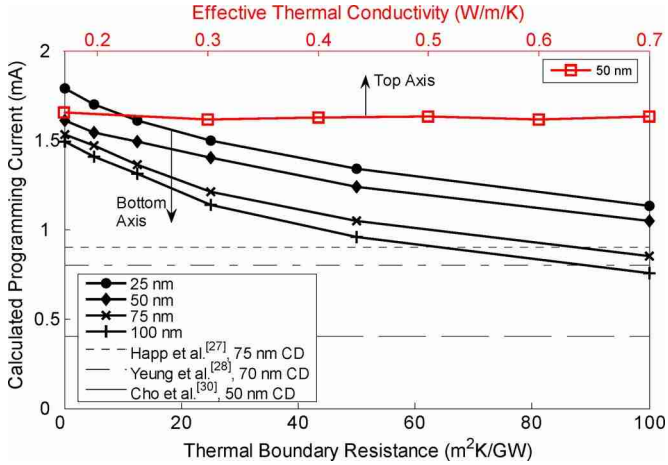

Fig. 3. Calculated programming current for different values of TBR with constant thermal conductivity (solid markers, bottom axis) and thermal conductivity with no TBR (hollow markers, top axis). Experimental data for cells with similar geometry and different BC–GST CDs are shown as dashed horizontal lines.

IV. Impact of the Thermal Boundary Resistance

The thermal and electrical resistances of the BC and phase-change region determine where the maximum temperature occurs. Cells that minimize programming current experience maximum temperature just above the GST–BC interface [25]. They have $R_{\rm BC,th} \approx R_{\rm PC,th}$ and $R_{{\rm BC},e} \approx R_{{\rm PC},e}$ [25]. $R_{\rm BC,th}$ and $R_{\rm PC,th}$ are the thermal resistances of the BC and phase-change region, respectively, and $R_{{\rm BC},e}$ and $R_{{\rm PC},e}$ are the electrical resistances of the BC and phase-change region, respectively. This work examines cells where the peak temperature occurs in the phase-change region above the interface, which is common for designs with $R_{\rm BC,th} \ll R_{\rm PC,th}$ and $R_{{\rm PC},e} < R_{{\rm BC},e}$. The results apply to cells with TBR in series with the minimum thermal resistance (commonly the BC). The TBR is in series with the BC resistance when the peak temperature occurs at or just above the interface. Electrical and thermal interface physics need to be included to fit experimental data in such a cell [8].

The temperature distribution during the reset pulse controls the phase distribution and resistance change of the cell [26]. The temperature at the edges of the BC must exceed the melting temperature for the amorphous region to cover the BC–GST interface, as is required for large electrical resistance changes [26]. Amorphization of the edges occurs at lower programming currents in cells with high lateral temperature uniformity.

Fig. 2 shows temperature distributions for a cell with no TBR and one with a TBR of 50 m^2 · K/W. TBR decreases the GST volume thermal resistance relative to the total thermal resistance between the active region and the ambient. This increases the lateral temperature uniformity in the GST and causes the location of maximum temperature to move toward the GST–BC interface. TBR, therefore, lowers the programming currents and the peak cell temperatures.

Fig. 3 shows how the spatial distribution of thermal resistances modifies the programming current. Solid markers indicate varying TBR with constant thermal conductivity. Programming currents decrease with TBR for all GST thicknesses. Introducing a TBR of 50 m^2 · K/GW reduces the programming current by $\sim$20% for the 25- and 50-nm GST layers and $\sim$30% for the 75- and 100-nm GST thicknesses. Lateral heat loss increases with GST thickness, decreasing the lateral temperature uniformity. Relative increases in lateral thermal resistance account for larger decreases in programming current in thicker films.

The hollow markers in Fig. 3 show that varying the GST effective thermal conductivity (with no TBR) has little effect on programming current. When $R_{\mathrm{BC,th}} \ll R_{\mathrm{PC,th}}$, very little heat is lost vertically through the GST, which renders the programming current relatively insensitive to the GST thermal conductivity [25]. Additionally, decreasing the thermal conductivity increases the thermal resistance isotropically. This decreases both the heat required to affect a given temperature change and the lateral temperature uniformity. Decreased lateral temperature uniformity requires larger programming currents to heat the edges above the melting temperature. This effect offsets the decrease in programming current caused by the larger thermal resistance.

V. Conclusion

This letter demonstrates that the TBR strongly influences the design and scaling of PCM devices. The predicted programming current decreases with TBR, owing to increased thermal confinement of the active region from the BC and increased lateral temperature uniformity in the GST.

Significant reductions in programming current are achievable by engineering thermal anisotropy into the active region of PCM devices. Deliberate introduction of interface disorder, Debye temperature mismatch, and weak bonding between the phase-change layer and surrounding metals may increase the TBR and reduce the programming current. Materials must be carefully chosen to increase the TBR without degrading electrical properties. Recent work shows that this is possible by adding fullerene layers at interfaces [30]. It may be possible to engineer thermal property anisotropy into the phase-change region by alternating low-conductivity phase-change layers with electronically compatible layers that have high in-plane thermal conductivity. Thermal property anisotropy can enhance vertical thermal confinement and lateral temperature uniformity, thereby reducing the programming current.

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