Understanding the switching mechanism of interfacial phase change memory

Cite as: J. Appl. Phys. 125, 184501 (2019); https://doi.org/10.1063/1.5093907
Submitted: 25 February 2019 . Accepted: 24 April 2019 . Published Online: 13 May 2019

Kye L. Okabe, Aditya Sood, Eilam Yalon, Christopher M. Neumann, Mehdi Asheghi, Eric Pop, Kenneth E. Goodson, and H.-S. Philip Wong

ARTICLES YOU MAY BE INTERESTED IN

Origin of resistivity contrast in interfacial phase-change memory: The crucial role of Ge/Sb intermixing
Applied Physics Letters 114, 132102 (2019); https://doi.org/10.1063/1.5088068

Engineering thermal and electrical interface properties of phase change memory with monolayer MoS₂
Applied Physics Letters 114, 082103 (2019); https://doi.org/10.1063/1.5080959

Tutorial: Brain-inspired computing using phase-change memory devices
Journal of Applied Physics 124, 111101 (2018); https://doi.org/10.1063/1.5042413
Understanding the switching mechanism of interfacial phase change memory

Kye L. Okabe,1 (✉) Aditya Sood,1,2,a) Eilam Yalon,1,b) Christopher M. Neumann,1 Mehdi Asheghi,2 Eric Pop,1,3 Kenneth E. Goodson,2,3 and H.-S. Philip Wong1,c)

AFFILIATIONS
1Department of Electrical Engineering, Stanford University, Stanford, California 94305, USA
2Department of Mechanical Engineering, Stanford University, Stanford, California 94305, USA
3Department of Materials Science and Engineering, Stanford University, Stanford, California 94305, USA

a)Present address: Stanford Institute for Materials and Energy Sciences, SLAC National Accelerator Laboratory, Menlo Park, California 94025, USA.

b)Present address: Department of Electrical Engineering, Technion—Israel Institute of Technology, Haifa 32000, Israel.

c)Author to whom correspondence should be addressed: hspwong@stanford.edu

ABSTRACT
Phase Change Memory (PCM) is a leading candidate for next generation data storage, but it typically suffers from high switching (RESET) current density (20–30 MA/cm²). Interfacial Phase Change Memory (IPCM) is a type of PCM using multilayers of Sb₂Te₃/GeTe, with up to 100× lower reported RESET current compared to the standard Ge₄Sb₂Te₅-based PCM. Several hypotheses involving fundamentally new switching mechanisms have been proposed to explain the low switching current densities, but consensus is lacking. Here, we investigate IPCM switching by analyzing its thermal, electrical, and fabrication dependencies. First, we measure the effective thermal conductivity (∼0.4 W m⁻¹ K⁻¹) and thermal boundary resistance (∼3.4 m² KGW⁻¹) of Sb₂Te₃/GeTe multilayers. Simulations show that IPCM thermal properties account only for an ∼13% reduction of current vs standard PCM and cannot explain previously reported results. Interestingly, electrical measurements reveal that our IPCM RESET indeed occurs by a melt-quench process, similar to PCM. Finally, we find that high deposition temperature causes defects including surface roughness and voids within the multilayer films. Thus, the substantial RESET current reduction of IPCM appears to be caused by voids within the multilayers, which migrate to the bottom electrode interface by thermophoresis, reducing the effective contact area. These results shed light on the IPCM switching mechanism, suggesting that an improved control of layer deposition is necessary to obtain reliable switching.

Published under license by AIP Publishing. https://doi.org/10.1063/1.5093907

I. INTRODUCTION
Phase change memory (PCM) is a class of emerging nonvolatile memory that combines several attractive properties, including random access, multilevel analog states,1 excellent scalability (down to approximately a few square nanometers),2–6 fast reading and writing,7,8 reasonable endurance (as high as ∼2 × 10¹² cycles9), and unipolar switching, while being compatible with back-end-of-the-line (BEOL) silicon processing. Its unique balance of cost-per-bit vs reading and writing time within the memory hierarchy makes PCM a leading candidate for storage class memory applications where cost and speed trade-offs between dynamic random-access memory (DRAM) and NAND flash are desired.10 Other compelling applications include neuromorphic analog computing systems, which have been demonstrated11,12 by leveraging device properties not available in conventional incumbent memories, such as static random-access memory (SRAM), DRAM, NAND flash, or hard disk drives.

The primary disadvantage of PCMs with respect to other nonvolatile memories is their high RESET current density, JRESET (and consequentially, RESET power and energy), which involves the switching phase change material layer (e.g., GST) to be heated above its melting temperature, Tm. For example, the energy required to RESET PCMs is greater than the typical energy required to charge interconnects for a random one-bit switch in a 1024 by 1024
memory array. On the other hand, other types of emerging nonvolatile memory, including resistive random-access memory (RRAM), conductive bridge random-access memory (CBRAM), and spin transfer-torque random-access memory (STT-MRAM), have at least a few demonstrations of switching energies below the interconnect charging energy. This indicates that PCMs still have an opportunity to effectively reduce system-level energy consumption by means of clever device-level engineering. For example, reducing the cell volume and reducing the programming pulse widths are two very effective ways to decrease the RESET energy by over an order of magnitude. However, these methods do not reduce \( J_{\text{RESET}} \), which is still around 20–30 MA/cm\(^2\) in typical PCMs. Such current densities cannot be matched by most memory selectors (Sec. 1 in the supplementary material), which are devices required to prevent unwanted leakage paths in memory arrays. Thus, selector devices for PCM would require separate patterning with a larger footprint, resulting in higher costs.

Recently, a new class of PCM called interfacial phase change memory (IPCM) has been reported with significant reduction of \( J_{\text{RESET}} \) from 35% to 99% compared to standard PCM cells (Sec. 2 in the supplementary material). IPCM has two distinguishing characteristics compared to conventional PCM: First, the structure consists of thinly stacked multilayers (generally a few nanometers each) of chalcogenides (Sb\(_2\)Te\(_3\) and GeTe being the most common) instead of a uniform chalcogenide layer (typically Ge\(_2\)Sb\(_2\)Te\(_5\), abbreviated as GST). Second, IPCMs are typically deposited at higher temperatures, ranging from 200 to 250 °C. Strategic spatial allocation of thermal resistance, as shown in Fig. 1(d), allows us to evaluate whether melt-quench RESET applies to IPCMs, without making specific assumptions involving the proposed mechanisms.

II. THERMAL ANALYSIS

Conventional PCMs RESET by a melt-quench process in which the switching phase change material layer (e.g., GST) is heated above \( T_{\text{m}} \) followed by a rapid quench that puts the GST in an amorphous state. Strategic spatial allocation of thermal resistances has previously been shown to play a key role in confining heat and reducing \( J_{\text{RESET}} \). Since IPCMs have a high cross-plane interfacial density, one possible cause of low \( J_{\text{RESET}} \) could be owed to enhanced thermal confinement due to lower effective thermal conductivity (=\( \kappa_{\text{eff}} \)) of the multilayer stack. We define \( \kappa_{\text{eff}} \) as the cross-plane thermal conductivity of the IPCM layers including “internal” Sb\(_2\)Te\(_3\)/GeTe thermal boundary resistances (TBR) but excluding “external” TBR to the top electrode (TE) and bottom electrode (BE), etc. To assess this hypothesis, we first measure \( \kappa_{\text{eff}} \) as a function of IPCM period thickness (=\( d \)), which allows us to estimate the contribution of the interfaces to the total thermal resistance. Then, we use finite element simulations to analyze how modifying \( \kappa_{\text{eff}} \) impacts the current and power density to heat a fixed volume within the memory cell. Since Joule self-heating is always present regardless of the actual switching mechanism, this allows us to evaluate whether melt-quench RESET applies to IPCMs, without making specific assumptions involving the proposed mechanisms.

Figure 1(a) shows a cross-sectional schematic of the IPCM samples used for thermal characterization, along with their process conditions (Sec. 3 in the supplementary material). Time domain thermoreflectance (TDTR) was used to measure \( \kappa_{\text{eff}} \) at room temperature (RT). Figure 1(b) reveals that \( \kappa_{\text{eff}} \) monotonically decreases with decreasing period thickness, suggesting that the interfacial thermal resistance is indeed significant compared to the volumetric resistances of the individual layers. To extract the TBR between Sb\(_2\)Te\(_3\) and GeTe, we plot the thermal resistance of a single period vs period thickness as shown in Fig. 1(c) and use a series resistor model (Sec. 4 in the supplementary material); the TBR is estimated to be \( \sim 3.4 \text{ m}^2 \text{ K GW}^{-1} \). This is noticeably lower than prior TBR studies of GST/TiN (\( \sim 26 \text{ m}^2 \text{ K GW}^{-1} \)) and GST/SiO\(_2\) interfaces (\( \sim 28 \text{ m}^2 \text{ K GW}^{-1} \)), potentially due to intermixing at the Sb\(_2\)Te\(_3\)/GeTe interface. Figure 1(d) plots the fractional contribution of the TBR to the unit period film thermal resistance, as a function of period thickness. We find that interfaces constitute nearly 50% of the thermal resistance in the thinnest period sample, \([4 \text{ nm Sb}_2\text{Te}_3;1 \text{ nm GeTe}]_{12}\). This sample has a thermal conductivity \( \kappa_{\text{eff}} \sim 0.4 \text{ W m}^{-1} \text{ K}^{-1} \); in comparison, literature values for Ge\(_2\)Sb\(_2\)Te\(_5\) films processed (200 °C) and measured (20 °C) at similar temperatures are close to \( \sim 0.5 \text{ W m}^{-1} \text{ K}^{-1} \), higher than that of IPCM. The lower \( \kappa_{\text{eff}} \) of the IPCM compared to GST-based PCM originates at least in part from the thermal resistance of the interfaces, as shown in Fig. 1(d).

The impact of \( \kappa_{\text{eff}} \) on \( J_{\text{RESET}} \) of IPCM was subsequently assessed by finite element simulations in Fig. 2(a). Voltage pulses with incremental amplitudes were applied across the top and bottom electrode until a constant fraction of the chalcogenide layer volume was heated above \( T_{\text{m}} \). Further details on simulation assumptions and methodologies are delineated in Sec. 5 in the supplementary material. Figure 2(b) shows the simulated \( J_{\text{RESET}} \) (blue circles) and RESET power density, \( P_{\text{RESET}} \) (orange crosses), as a function of \( \kappa_{\text{eff}} \) over \( \kappa_{\text{GST}} \). From these simulations, we deduce decreasing \( \kappa_{\text{eff}} \) from GST to the best case (lowest \( \kappa_{\text{eff}} \)) IPCM results in only \( \sim 13\% \) reduction of \( J_{\text{RESET}} \) and \( \sim 17\% \) reduction of \( P_{\text{RESET}} \). From a purely thermal standpoint, our simulations estimate that to reduce \( J_{\text{RESET}} \) by \( \sim 10 \times \), \( \kappa_{\text{eff}} \) must be reduced by \( \sim 100 \times \), which is unphysical because it is much less than the thermal conductivity of dry air (\( \sim 0.023 \text{ W m}^{-1} \text{ K}^{-1} \)).

Considering the magnitude of previously reported \( J_{\text{RESET}} \) reductions shown in Sec. 2 in the supplementary material (100x reduction as an example), we conclude that the modest difference in thermal properties alone cannot explain the observed \( J_{\text{RESET}} \) reductions. We note that due to the lack of Sb\(_2\)Te\(_3\), GeTe, and Sb\(_2\)Te\(_3\)/TiN interface temperature-dependent electrical resistivity studies above room
temperature,\textsuperscript{44} our simulations assumed electrical resistivity of GST\textsuperscript{45} and GST/metal interfaces.\textsuperscript{46} If $T_m$ of Sb$_2$Te$_3$ or GeTe were lower than GST and had higher electrical resistivities, it might be possible to reduce $J_{\text{RESET}}$ even further, but since bulk $T_m$ values are comparable or higher (GeTe: $\sim$720 °C, Sb$_2$Te$_3$: $\sim$620 °C, and GST: $\sim$620 °C), we do not expect 100-fold $J_{\text{RESET}}$ reduction even with these modifications.

III. ELECTRICAL ANALYSIS

Next, to assess IPCM electrical characteristics, we fabricate and test mushroom-type memory cells with 80 nm diameter TiN bottom electrode (BE) and [4 nm Sb$_2$Te$_3$:1 nm GeTe]$_{10}$ stack (with Sb$_2$Te$_3$ as the starting layer contacting the BE), as detailed in Sec. 3 in the supplementary material. Reference PCM cells with 50 nm of Ge$_2$Sb$_2$Te$_5$ and identical BE conditions were also fabricated for comparison. The chalcogenide layers for both PCM and IPCM devices were sputtered at 200 °C in Ar ambient with a pressure of 4 mTorr. Figure 3(a) shows DC read resistance vs current measurements (electrical measurement setup and methodologies are described in Sec. 6 in the supplementary material). Well-behaved PCMs have $J_{\text{RESET}}$ $\sim$ 25 MA/cm$^2$, while IPCMs $J_{\text{RESET}}$ is $\sim$30 MA/cm$^2$. IPCMs had a noticeably higher cycle-to-cycle variation (Sec. 7 in the supplementary material). Interestingly, we were also able to measure low $J_{\text{RESET}}$ IPCMs from a different device on the same chip. The low $J_{\text{RESET}}$ device degraded soon after and we were
unable to perform further measurements, an observation we will return to below. Figure 3(b) shows $R_{\text{read}}$ vs $R_{\text{trans}}$, where $R_{\text{trans}} = \frac{V_{\text{applied}} - V_{\text{scope}}}{I}$ and $I = \frac{V_{\text{scope}}}{50\ \Omega}$.

$$R_{\text{trans}}$$ is the resistance of the device under test (DUT), while the voltage pulse is being applied. For the reference PCM, because the BE diameter is larger than the GST thickness, the entire stack between the top and the bottom electrode gets heated during RESET. Due to the temperature dependence of the electrical resistivity of GST, the resistance of the PCM must go through a low transient resistance state before reaching a higher final DC read resistance state. Interestingly, we find IPCMs following the same trend, suggesting a melt-quench based RESET.

To verify that the low $R_{\text{trans}}$ in IPCMs originates from a thermal process rather than from electric fields, pulsed measurements as a function of pulse fall time ($t_{\text{fall}}$) were performed using a fixed voltage amplitude shown in Fig. 3(c). We find both PCM and IPCM $R_{\text{read}}$ are dependent on $t_{\text{fall}}$ and conclude that both exhibit melt-quench based RESET. Importantly, although the RESET mechanism of IPCMs has been debated, to the best of our knowledge, there have been no experimental demonstrations of nonvolatile DC RESET of IPCMs to date. The one close exception is a demonstration of volatile selectorlike DC RESET. Since a dependence on rapid cooling is the defining characteristic of melt-quench based RESET, we anticipate that if a fundamentally new mechanism exists, it should be possible to demonstrate slow cooling RESET (i.e., DC RESET).

IV. PROCESS ANALYSIS

To gain additional insight, IPCM devices were cross-sectioned and imaged by scanning electron microscopy (SEM). Figure 4(a) shows an example of an as-fabricated device that has not been electrically probed, showing defects including surface roughness and voids within the IPCM layer. The distribution of voids is stochastic, and depending on the specific device and cutting angle, images without voids were also obtainable (example shown in Fig. 5). Figures 4(b) and 4(c) show conceptual diagrams of a possible cause of $J_{\text{RESET}}$ reduction when a void is present near the BE. Initially, the void is static because there are no driving forces on the surrounding atoms. Once a voltage pulse is applied across the TE and BE, the current generates a hot spot with a radial temperature gradient above the BE due to Joule heating of the chalcogenide/BE contact. Because hot atoms move much faster than the slow atoms, this causes a net flux of atoms from the hot region toward cold regions with voids. This process can effectively be seen as voids being attracted toward the region above the BE in the presence of a

![Fig. 3](image_url)

**FIG. 3.** (a) $R_{\text{read}}$ vs $I$ of relatively well-behaved PCM (green) and IPCM (brown). IPCMs with low $J_{\text{RESET}}$ currents (purple) were also measured from the same chip (processed through the same run) as the brown device, but they had poor endurance. (b) $R_{\text{read}}$ vs $R_{\text{trans}}$. $R_{\text{trans}}$ was averaged over the duration of the pulse width (100 ns). Similar trends hint that both PCM and IPCM RESET are based on a melt-quench process. (c) $R_{\text{read}}$ vs $t_{\text{fall}}$, indicating both PCM and IPCM RESET by a melt-quench process. The voltage amplitude was fixed at 1.2 V for PCMs and 1.5 V for IPCMs. Ten measurements were performed for each fall time for reproducibility.

![Fig. 4](image_url)

**FIG. 4.** (a) Cross-sectional SEM of an as-processed IPCM device prior to electrical probing, showing voids within the IPCM. (b) and (c) Conceptual diagrams illustrating possible $J_{\text{RESET}}$ reduction mechanism: temperature gradients during RESET cause atomic diffusion from above the BE (hot region) to colder regions with voids (i.e., thermophoresis). Consequently, nearby voids are attracted above the BE, reducing the effective device size, thus reducing the apparent $J_{\text{RESET}}$. 

Published under license by AIP Publishing.
Since PCMs are not filamentary devices, the RESET current is roughly proportional to the chalcogenide/BE contact area. Hence, once the contact area is reduced by the voids, the RESET current is expected to reduce. This mechanism also explains why we observed significant $J_{\text{RESET}}$ variation between IPCM devices. If a void is not present within an accessible range of the temperature gradient, devices RESET in a well-behaved manner at consistent voltages, but with relatively high $J_{\text{RESET}}$ due to no IPCM/BE contact area reduction.

Finally, control tests were performed to further understand the dependence of IPCM morphology on deposition temperature. Figure 5 shows top-view and cross-sectional SEMs of TiN/IPCM/BE test structure arrays. The cross-sectional SEMs have an additional Pt layer on the surface deposited in situ during FIB sample preparation. When deposited at room temperature, IPCM films were very conformal, with the BE morphology visibly carrying over to the surface. At 200 °C deposition temperature, surface roughness and voids become visible, clearly degrading the integrity of the film. As mentioned previously, the void distribution is stochastic. In contrast to Fig. 4(a), Fig. 5(e) shows an example of a device with no apparent nearby voids. At 250 °C, minimal IPCM deposition is observed, with the TiN TE layer depositing on small IPCM islands on the surface causing flaking. The deposition time of the stack was kept constant for all three films. Similar morphological trends dependent on deposition temperature were observed with GST as well, and are shown in Sec. 8 in the supplementary material. Additional control tests are presented in Sec. 9 in the supplementary material showing thermal instability of solid-phase chalcogenides at elevated temperatures (200–250 °C) due to sublimation, which is likely related to void formation. One possible path toward avoiding these issues may be to deposit IPCMs at room (or lower) temperatures, followed by deposition of a capping layer, and subsequent annealing to prevent sublimation. Prior work has shown that intermixing of Sb$_2$Te$_3$/GeTe becomes problematic at 400 °C annealing, but further investigation remains as future work.

V. CONCLUSION

In summary, the contributions of this work are the following: (1) thermal characterization of IPCM films including period-dependent $\kappa_{\text{eff}}$ (as low as $\sim0.4 \text{ W m}^{-1} \text{K}^{-1}$) and TBR of the Sb$_2$Te$_3$/GeTe interface ($\sim3.4 \text{ m}^2 \text{ K GW}^{-1}$); (2) finite element simulations showing IPCM thermal properties alone cannot account for substantial ($\sim100\times$) $J_{\text{RESET}}$ reductions; (3) electrical measurements showing both PCM and IPCM exhibit melt-quench-based RESET, and pointing out that no prior work has shown nonvolatile DC RESET; (4) discovery of randomly generated voids within chalcogenide films deposited at high ($\sim200$ °C) temperatures; (5) proposing an alternate mechanism for the large apparent reduction of $J_{\text{RESET}}$ in IPCM based on our findings and well-known physics; (6) control tests showing sublimation of Ge$_2$Sb$_2$Te$_5$ and Sb$_2$Te$_3$ at elevated ($\sim250$ °C) temperatures, possibly related to void formation; and (7) various other supplementary content, including surveys of IPCM RESET current density and selector ON current density.

SUPPLEMENTARY MATERIAL

See the supplementary material for (1) survey of selector ON current densities, (2) survey of IPCM $J_{\text{RESET}}$, (3) PCM and IPCM film deposition conditions, (4) Sb$_2$Te$_3$/GeTe thermal boundary resistance extraction, (5) finite element simulation assumptions and methodology, (6) electrical measurement setup, (7) PCM and IPCM cycle-to-cycle RESET variation, (8) morphology of PCM dependent on deposition temperature, (9) control tests with varying postdeposition annealing conditions showing sublimation of Sb$_2$Te$_3$ and Ge$_2$Sb$_2$Te$_5$, and (10) sputtering chamber cooling and pumping rates.

ACKNOWLEDGMENTS

This work was supported in part by the National Science Foundation (NSF) [ECCS-1709200 Collaborative Research: Nanopatterning and temporal control of phase-change materials for reconfigurable photonics and EEC-1449548 Engineering Research Center on Power Optimization of Electro-Thermal Systems (POETS)] as well as the member companies of the Stanford Non-Volatile Memory Technology Research Initiative (NMTRI) and the Semiconductor Research Corporation (SRC). Part of this work was performed at the Stanford Nanofabrication Facility (SNF) and Stanford Nanofabrication Shared Facilities (SNSF), supported by the National Science Foundation under award ECCS-1542152. The authors thank Jim McVittie for lab assistance and valuable discussions.