Temperature-Dependent Thermal Properties of Phase-Change Memory Electrode Materials

Elah Bozorg-Grayeli, John P. Reifenberg, Matthew A. Panzer, Jeremy A. Rowlette, and Kenneth E. Goodson

***Abstract*—The programming current required to switch a phase-change memory cell depends upon the thermal resistances in the device. In many designs, significant heat loss occurs through the electrode. This letter investigates the thermal properties of a multilayer electrode stack. This material offers greater thermal resistance than single-material electrodes due to the presence of multiple thermal boundary resistances (TBRs), reducing heat loss from the device and potentially lowering the programming current. Picosecond time-domain thermoreflectance interrogates the temperature-dependent thermal conductivity of three as-deposited and postannealed electrode materials: carbon, titanium nitride, and tungsten nitride. These data are used to extract the temperature-dependent, as-deposited, and postannealed TBR in two multilayer electrode stacks: carbon–titanium nitride and tungsten–tungsten nitride. The C–TiN stacks demonstrate an as-deposited TBR of 4.9 m^2K/GW, increasing to 11.9 m^2K/GW postanneal. The W–WN_x stacks demonstrate an as-deposited TBR of 3.9 m^2K/GW, decreasing to 3.6 m^2K/GW postanneal. These resistances are equivalent to electrode films with thickness on the order of tens of nanometers.**

***Index Terms*—Electrode materials, nonvolatile memory, phase-change memory (PCM), thermal boundary resistance (TBR), thermal conductivity.**

I. Introduction

THE SWITCHING behavior of a phase-change memory (PCM) cell is dependent upon several factors, including: device size [1], applied fields [2], and the temperature gradient developed at the electrode–device interface [1]. The latter property is influenced by the thermal resistances of the device. Reifenberg *et al.* demonstrated through coupled electrical–thermal simulations that the programming current of a $Ge_2Sb_2Te_5$ (GST)-based device decreases as the total thermal resistance of the cell increases [1]. Furthermore, Karpov and Kostylev showed that much of the heat generated during GST cell switching occurs in the GST bulk and at the electrode interface [3]. For this reason, one of the goals in PCM thermal design is to minimize heat loss from the cell. Heat loss through the electrode dominates in many PCM cell geometries. Electrode materials with low thermal conductivities and larger thermal boundary resistance (TBR) can therefore reduce heat loss in PCM cells. The TBR is a function of several properties, including phonon spectra and interface quality [4], [5]. Previous work shows data for GST–electrode TBR in the range of 5–50 m^2K/GW [6], [7]. However, as shown in [6], electrodes with low thermal conductivity may not have high TBR. For electrode materials such as C, Ti, and TiN, TBR becomes comparable to intrinsic thermal resistance when their thicknesses approach $\sim$30 nm [6]. As such, there may not be a single composition electrode material which is suitable for use at multiple thickness scales. Therefore, designers must consider new ways to utilize the GST–electrode TBR while increasing the intrinsic electrode thermal resistance.

In order to minimize the heat loss from a GST cell, the authors proposed a multilayer electrode stack. The presence of the material interfaces in these electrodes would contribute significantly to the total thermal resistance of the stack. Furthermore, the bottom film of the stack can be chosen to maximize the GST–electrode TBR, which impedes heat loss from the PCM cell and reduces the programming current [1].

This letter measures and assesses the importance of TBR in three prospective PCM electrode materials. Samples are measured as-deposited and after a 5-min anneal at 400 °C. A picosecond thermoreflectance setup interrogates the thermal properties of the samples in an optical access oven. Multilayer stacks of electrode materials are measured to determine the electrode–electrode TBR for C–TiN and W–WN_x. Temperature-dependent measurements of all samples determine the thermal conductivity and TBR in the range of 25 °C–400 °C.

II. Experimental Method

A picosecond time-domain thermoreflectance (TDTR) setup extracts the thermal properties of these materials at different ambient temperatures. TDTR is a well-established optical measurement technique that uses delayed pump and probe laser pulses to heat a sample and interrogate its temperature response [8], [9]. Since metals exhibit linear changes in reflectivity with temperature for small temperature changes, this technique extracts a normalized temperature decay for a heated metal transducer film on a stack of thin film materials [10]. An optical access oven controls the temperature of the sample from 30 °C to 400 °C. The oven maintains a vacuum to prevent transducer oxidation.

Manuscript received May 2, 2011; revised May 23, 2011; accepted May 31, 2011. Date of publication June 27, 2011; date of current version August 24, 2011. This research was supported in part by Intel, by the Air Force Office of Scientific Research, and by a National Defense Science and Engineering Graduate Fellowship, 32 CFR 168a. The review of this letter was arranged by Editor K. De Meyer.

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Digital Object Identifier 10.1109/LED.2011.2158796

The Feldman algorithm for heat flow through a multilayer stack fits the decay curves [11], [12]. The model considers 3-D rotationally symmetric heat deposition at the transducer–ambient interface. The intrinsic electrode thermal conductivity, transducer–electrode TBR, and electrode–silicon TBR are used as fitting parameters. A nonlinear curve-fitting algorithm determines the best fit set of parameters for the single-layer electrode samples.

All samples were deposited using magnetron sputtering. Tungsten deposition utilized dc power and argon plasma. Carbon deposition used pulsed-dc power at 90 kHz with argon plasma. TiN and WN_x were both deposited using dc power and reactive argon–nitrogen plasma with pure titanium and pure tungsten sputtering targets, respectively. The multilayer samples underwent similar deposition, without air breaks in the C–TiN or W–WN_x layers.

Single-layer samples of each film ranged in thickness from 25 to 100 nm. The multilayer stacks consisted of five periods of W/WN_x (70 nm/100 nm) or C/TiN (11 nm/110 nm). A 50-nm aluminum layer acts as the transducer film. Annealed samples were held for 5 min at 400 °C, with ramp-up taking less than 60 min and cooldown taking less than 30 min.

For the film compositions in this letter and at time scales below ∼400 ps, the thermal decay time of the transducer layer is dependent on the heat capacitance of the film and the Al–electrode TBR such that, at short times, $\tau \sim R_{\mathrm{Al-electrode}} C_{\mathrm{Al}}$, where C_{Al} is the volumetric heat capacity multiplied by the aluminum film thickness. During this time period, the thermal decay behavior is sensitive to only the transducer–electrode TBR. As a result, the TBR is uniquely separable from the electrode thermal conductivity [7]. For the multilayer samples, the model fits an effective thermal resistance for each individual electrode layer. For the W–WN_x sample, this becomes an effective thermal conductivity for each electrode material type. The total thermal resistance of a W–WN_x pair is calculated, and the intrinsic thermal resistances of the W–WN_x and W layers are subtracted out, leaving a resistance equal to twice the W–WN_x TBR. For W, the intrinsic conductivity is obtained by scaling the bulk conductivity to account for boundary scattering. For the C–TiN sample, since the carbon layers are very thin, the model treats the stack as several layers of TiN with equal TBR between each layer. This TBR term includes the intrinsic carbon resistance and the C–TiN TBR. Subtracting out the intrinsic C thermal resistance leaves a resistance equal to twice the C-TiN TBR.

III. Results and Discussion

All single-layer samples exhibit a decrease in total area-normalized thermal resistance ($R_{\mathrm{total}} = L_{\mathrm{electrode}}/k_{\mathrm{electrode}} + R_{\mathrm{Al-electrode}} + R_{\mathrm{electrode-si}}$) as temperature rises, with the as-deposited samples showing significant temperature hysteresis. After separating out the TBR terms from the total resistance, only the titanium nitride sample shows an increase in intrinsic thermal conductivity after annealing (see Fig. 1). This may be due to a decrease in defect density within the TiN film, resulting in a higher phonon mean free path. In all other cases, the thermal resistance decreases

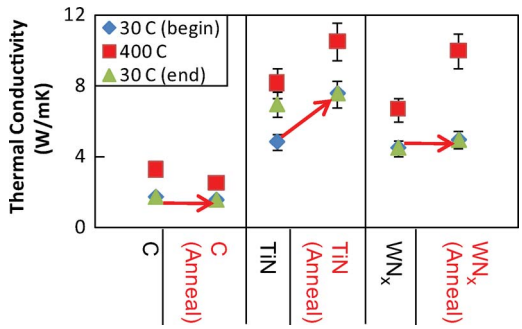

Fig. 1. Thermal conductivity of the single-layer electrode samples. The red arrows indicate the change of room temperature conductivity between the as-deposited and postannealed samples. Error bars are due to uncertainty in sample thickness.

TABLE I
TBRs of Single-Layer Stacks

Film	$R_{\mathrm{Al-electrode}}$ (m^2K/GW)	$R_{\mathrm{Al-electrode,annealed}}$ (m^2K/GW)	$R_{\mathrm{electrode-Si}}$ (m^2K/GW)	$R_{\mathrm{electrode-Si,annealed}}$ (m^2K/GW)
C	4.3	3.9	2.3	2.0
TiN	1.1	1.7	3.6	3.9
WN_x	4.4	3.3	8.8	6.6

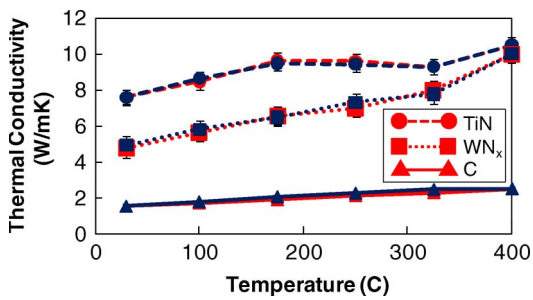

Fig. 2. Thermal conductivity of the postannealed single-layer samples. The (light) red points indicate the heating curve, and the (dark) blue points indicate the cooling curve. Hysteresis effects are not visible for these samples.

due to annealing of the material interfaces (see Table I). Conducting the same measurement on the annealed samples demonstrates that the hysteresis effect is no longer visible (see Fig. 2). This indicates that the 5-min anneal time is sufficient to promote temperature stability of single-layer electrode thermal properties. The data shown in Figs. 1 and 2, as well as Table I, form the fitting parameters for the multilayer stacks. Error due to signal noise is small. As a result, electrode thickness uncertainty controls the error bars.

Both annealing time and temperature impact the thermal conductivity of the TiN and WN_x films. Annealing these samples before conducting high-temperature measurements results in a higher thermal conductivity at 400 °C than for the as-deposited films. This may be due to the annealed samples spending a greater total amount of time at elevated temperature. As a result, the annealed samples would have a lower dislocation density than the as-deposited samples, resulting in a higher thermal conductivity.

For the multilayer stacks, W–WN_x exhibited a small decrease in TBR due to annealing, from 3.9 to 3.6 m^2K/GW, comparable to roughly 20 nm of the WN_x film at room temperature (see Fig. 3). The annealed sample showed no temperature

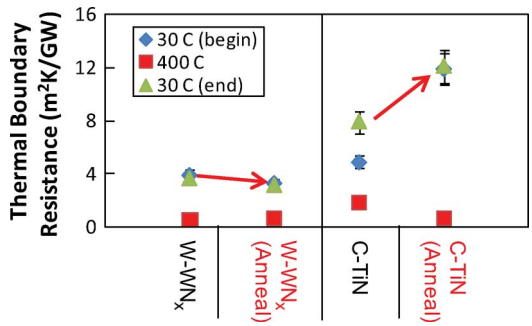

Fig. 3. TBR electrode multilayer samples. The red arrows indicate the change of room temperature TBR between the as-deposited and postannealed samples. Error bars are due to uncertainty in the thickness of the electrode films.

hysteresis. The C–TiN multilayer, on the other hand, showed a significant increase in the apparent TBR after annealing, from 4.9 to 11.9 m^2K/GW. This is comparable to roughly 40 and 100 nm, respectively, of TiN at room temperature. Since the carbon layers were roughly 10 nm thick, interdiffusion from the TiN layers at high temperature may have resulted in a highly disordered film rather than a solid interface [13]. Interdiffusion in this disordered layer would significantly decrease the phonon mean free path due to impurity scattering, resulting in a lower thermal conductivity. The measured thermal conductivity is therefore representative of an elementally heterogeneous film. The absence of a sharp material interface in this film implies the need for careful interpretation of the extracted TBR. For this reason, Fig. 3 defines an apparent TBR using the intrinsic carbon thermal conductivity determined from the single-layer samples.

Although the electrode–electrode TBR decreases at high temperature, it remains an important contributor to electrode thermal resistance. For annealed W–WN_x, the TBR at 400 °C (0.5 m^2K/GW) is equivalent to 5 nm of WN_x at the same temperature. For annealed C–TiN, the TBR at 400 °C (0.6 m^2K/GW) is equivalent to 6 nm of TiN at the same temperature. In both cases, the TBR at high temperature accounts for ∼10% of the total resistance of the multilayer stack ($R_{\text{total,multilayer}} = L_{\text{electrode},1}/k_{\text{electrode},1} + L_{\text{electrode},2}/k_{\text{electrode},2} + 2R_{\text{electrode},1-\text{electrode},2}$).

IV. Conclusion

This letter demonstrates that multilayer stacks exhibit significant increases in thermal resistance relative to single-material electrodes. This additional resistance can reduce the programming current in many PCM cell geometries. Specifically, C–TiN electrode stacks offer both high intrinsic resistance and high TBR. Annealing gives control over the thermal resistances of the PCM cell. It may also lead to further incorporation of titanium and nitrogen into the carbon layer. This makes it difficult to define a solid material interface. As such, the results presented here define an apparent boundary resistance based on the anticipated intrinsic thermal resistance of the carbon layer.

The improved thermal properties of these materials alone will not necessarily lead to a reduction in programming current. The PCM cell geometry and dimensions will influence whether the electrode material is the dominant path for heat loss from the GST cell. The device designer may choose to alter the periodicity of these multilayer materials in order to control the electrode thermal resistance. By using such design techniques with the aforementioned materials, one can control the thermal decay time of the memory cell and, therefore, the programming current.

Acknowledgment

The authors would like to thank K.-W. Chang and his colleagues at Intel Corporation for their assistance on this letter.

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